

EG060K&EG120K Series

Reference Design

LTE-A Module Series

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About the Document

Revision History

Version	Date	Author	Description
-	2021-06-11	David WANG	Creation of the document
1.0	2022-04-07	Elliot CAO	First official release
1.1	2024-06-24	Murray YIN/ Lewis PENG	<ol style="list-style-type: none">1. Added the related information of EG060K-NA/LA/JP/GT and EG120K-NA/LA/JP.2. Added a note on avoiding abnormal RF functions caused by current sink on the module's pins (Sheet 1).3. Reserved DC isolation capacitors at the ANT0/1/2/3 ports and added a note for explanation (Sheet 10).

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1 Reference Design

1.1. Introduction

This document provides the reference design for EG060K&EG120K series modules. The reference design includes block diagram, power system block diagram, module interfaces, host interfaces, power supply designs, (U)SIM and UART designs, SLIC design, SD card design, antenna interface design, indicators and test points and so on.

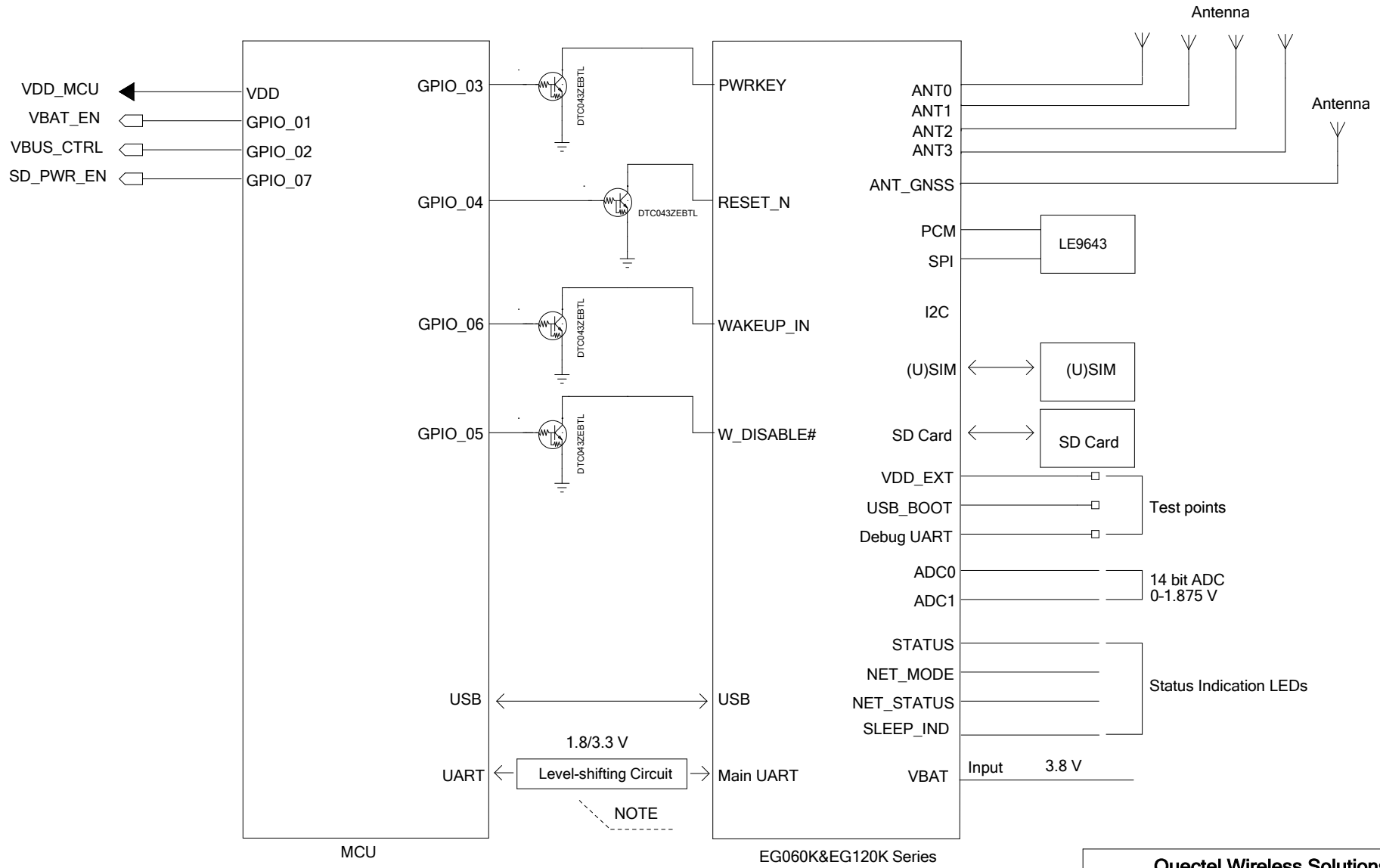
Table 1: Applicable Modules

Module Series	Module
EG060K	EG060K-EA
	EG060K-NA
	EG060K-LA
	EG060K-JP
	EG060K-GT
EG120K	EG120K-EA
	EG120K-NA
	EG120K-LA
	EG120K-JP

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



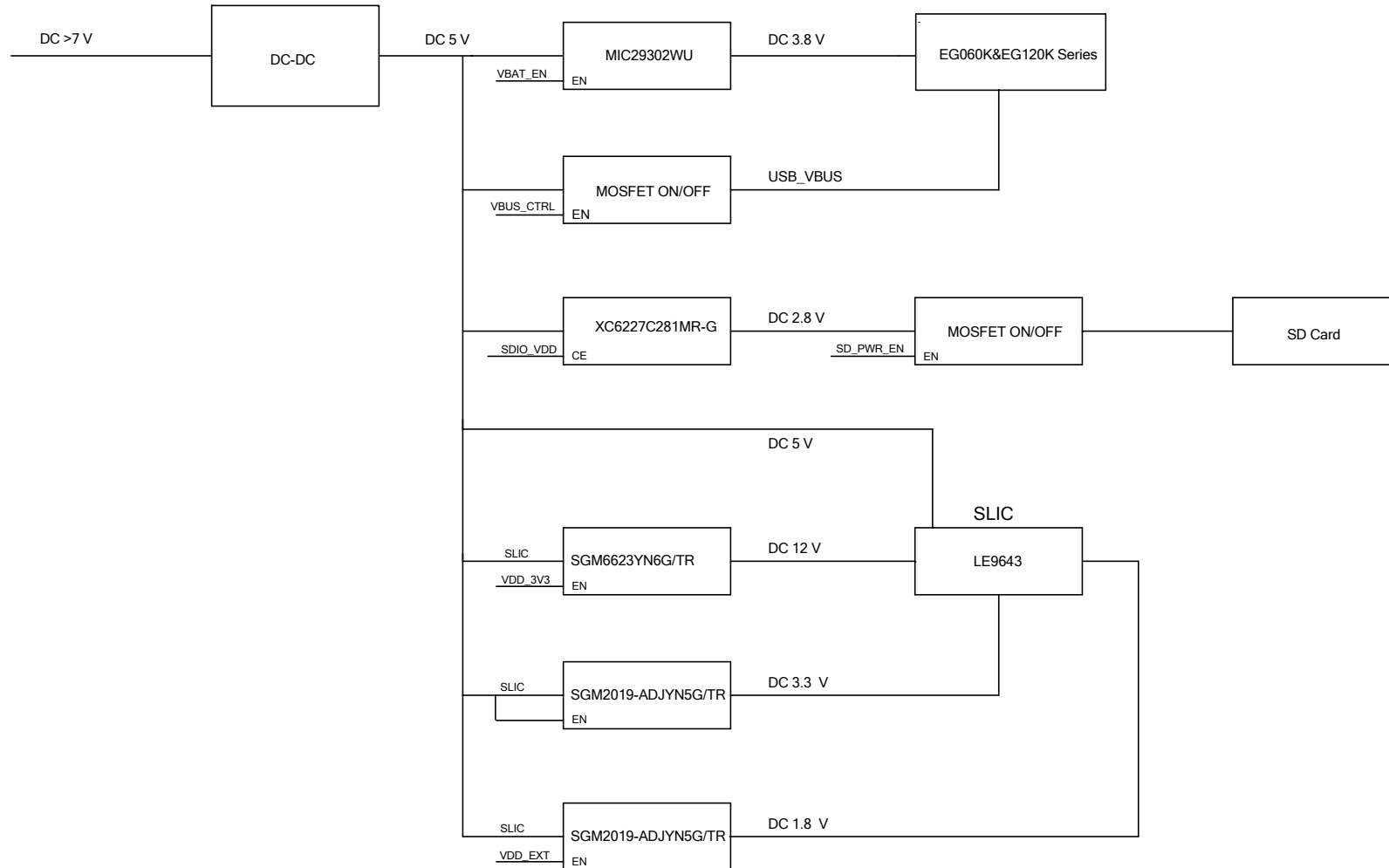
NOTE:

1. A level-shifting circuit with a triode or a voltage-level translator TXS0108EPWR provided by Texas Instruments (TI) is recommended.
2. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on.

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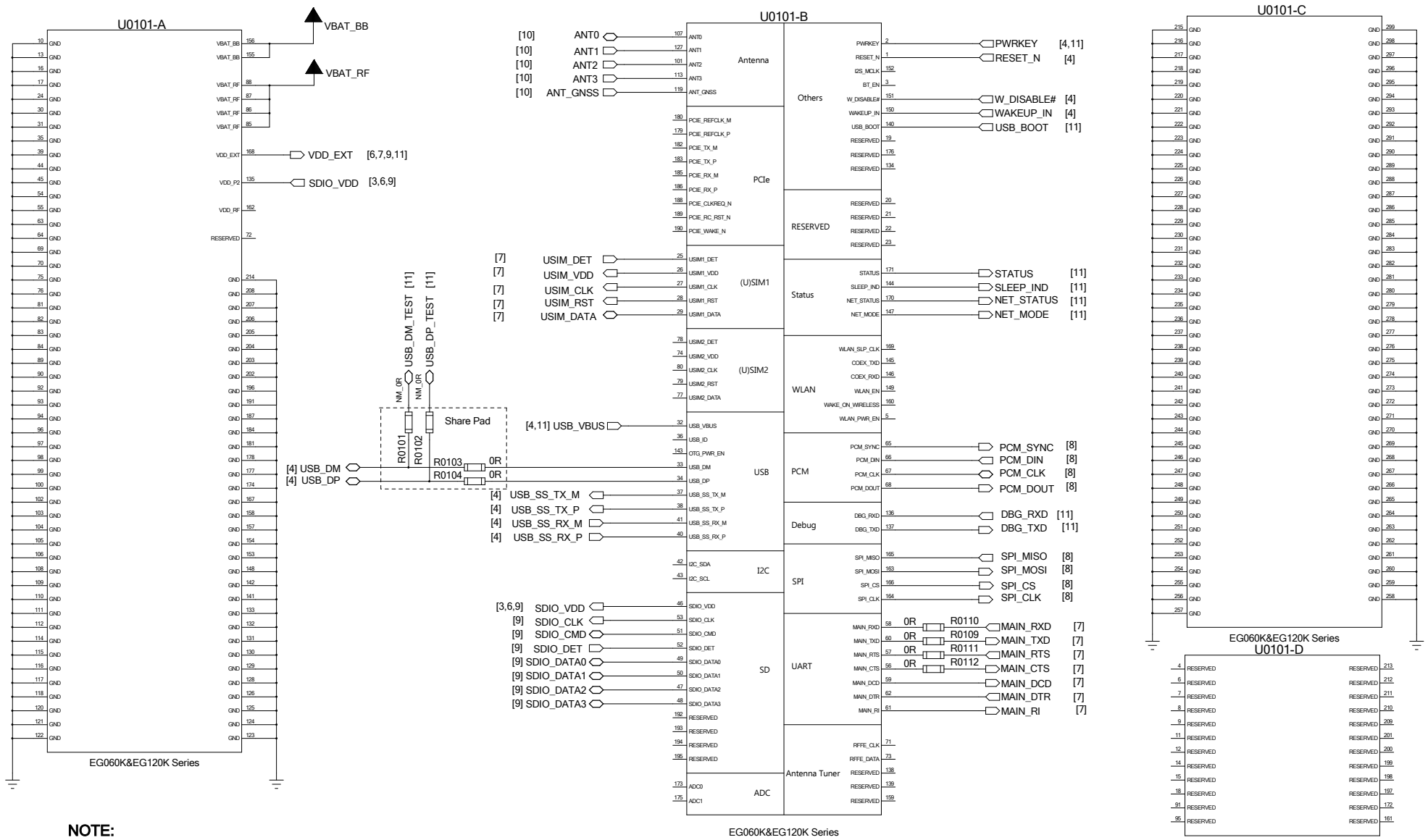
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Power System Block Diagram



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Module Interfaces

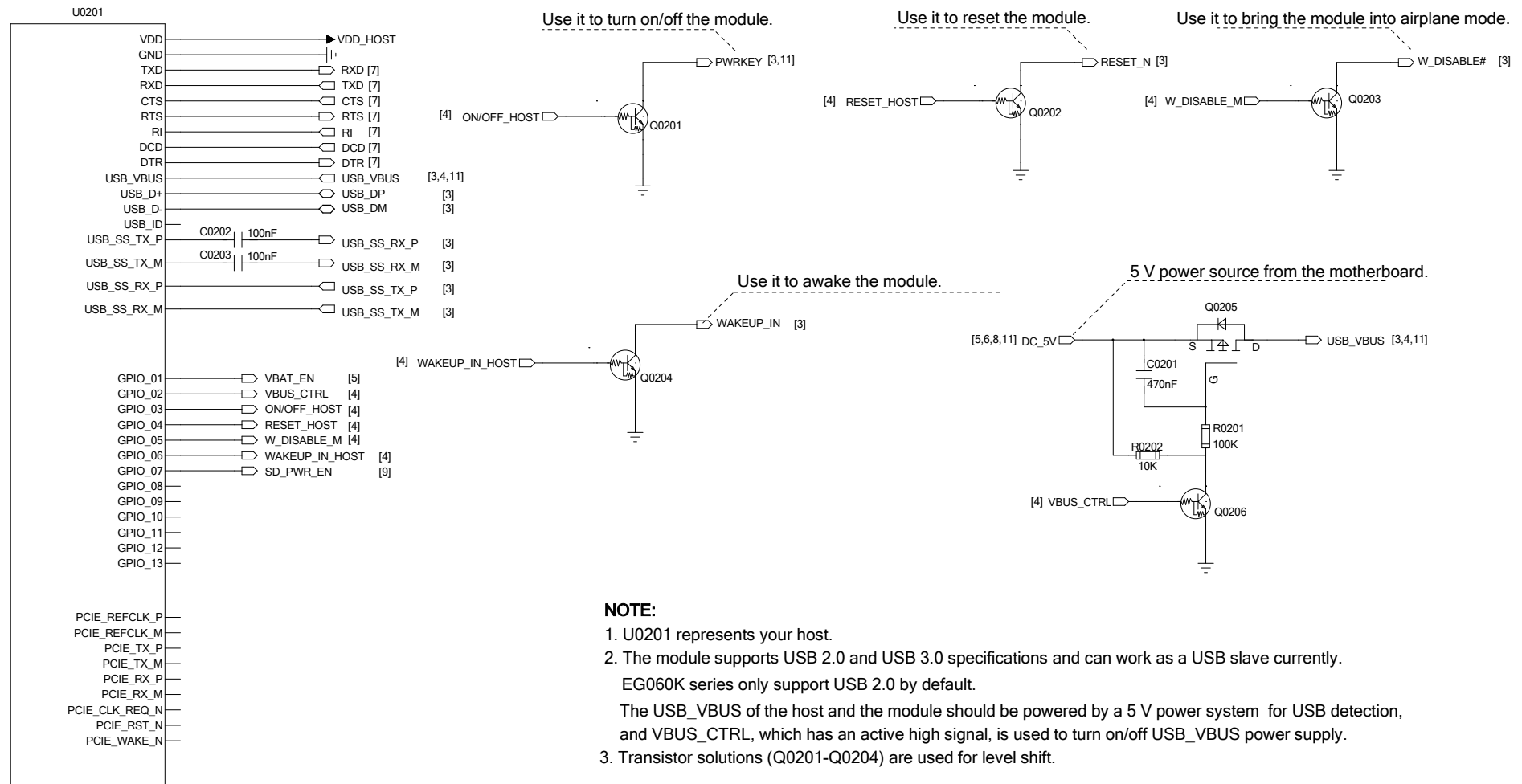


NOTE:

1. ADC pins cannot be directly connected to the power supply. The input voltage ADC pins should not exceed 1.875 V.
2. It is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the stub length of USB test signals.
3. Keep all RESERVED and unused pins unconnected, and all GND pins connected to the ground network.
4. If an SD card is used, connect VDD_P2 to SDIO_VDD. If an eMMC is used or the SDIO interface is unused, connect VDD_P2 to VDD_EXT.

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Host Interfaces



NOTE:

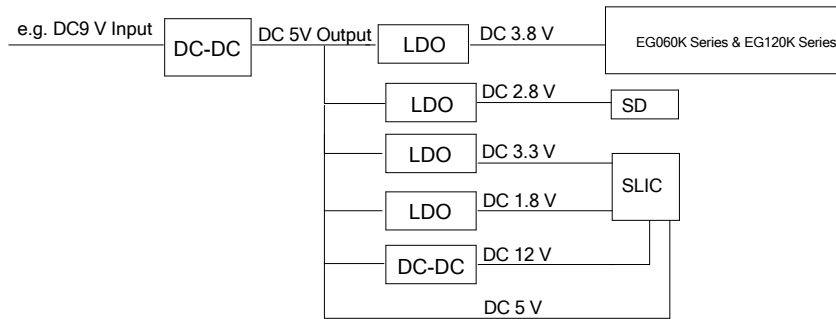
1. U0201 represents your host.
2. The module supports USB 2.0 and USB 3.0 specifications and can work as a USB slave currently.
 EG060K series only support USB 2.0 by default.
 The USB_VBUS of the host and the module should be powered by a 5 V power system for USB detection, and VBUS_CTRL, which has an active high signal, is used to turn on/off USB_VBUS power supply.
3. Transistor solutions (Q0201-Q0204) are used for level shift.

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Power Supply (Part 1)

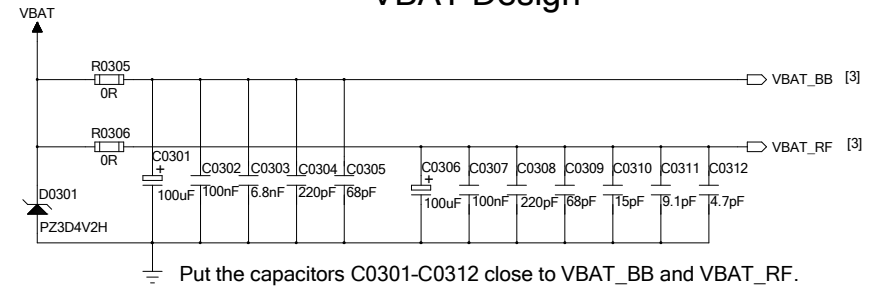
DC-DC Application



NOTE:

When the input voltage is above 7 V, a DC-DC converter should be used to convert the high input voltage to a 5 V output, then the LDOs will generate typical voltages of 3.8 V, 2.8 V, 3.3 V and 1.8 V, and the DC-DC will generate a 12 V typical voltage.

VBAT Design

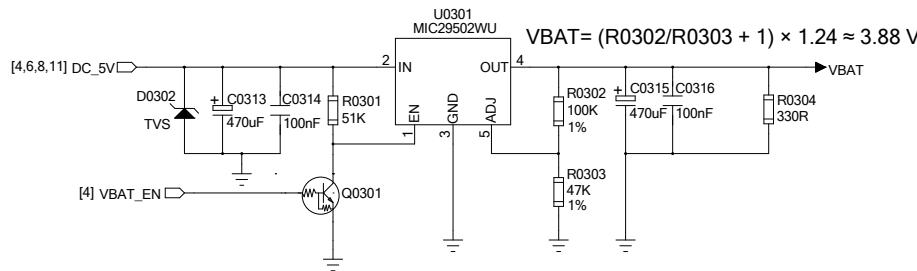


Put the capacitors C0301-C0312 close to VBAT_BB and VBAT_RF.

NOTE:

1. The power supply must be able to provide sufficient current up to 2 A at least.
2. VBAT should be routed in star topology to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3-4.4 V.

LDO Application



NOTE:

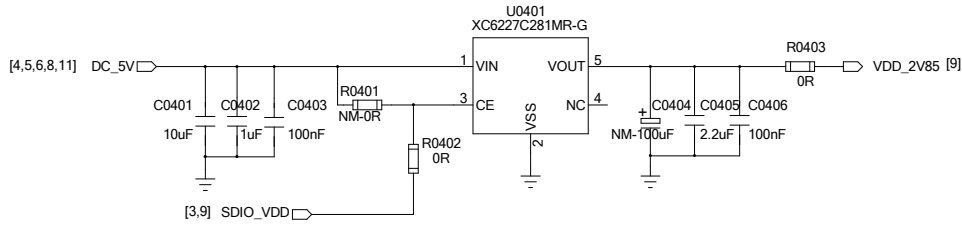
The load current of MIC29502WU is recommended to be greater than 10 mA.

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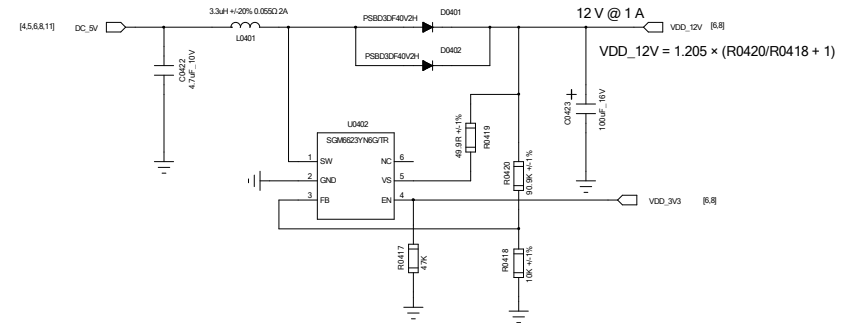
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Power Supply (Part 2)

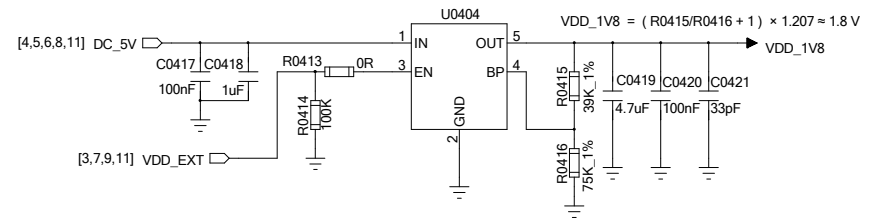
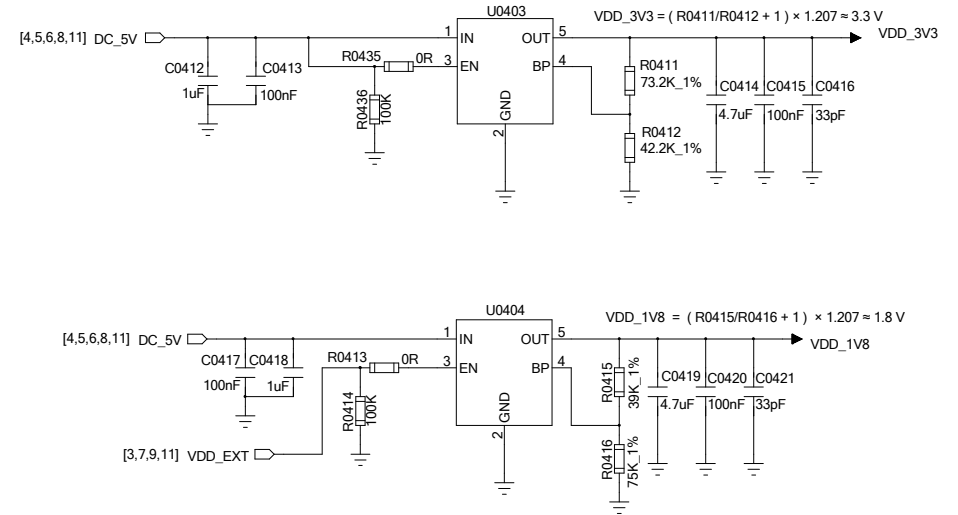
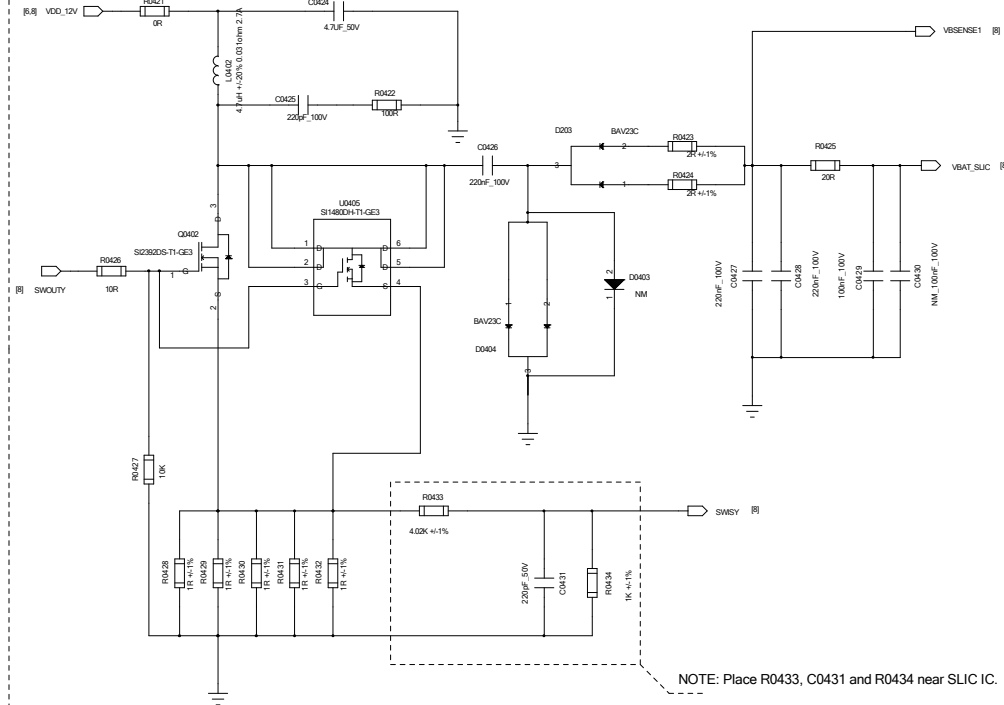
Power Supply for SD Card



Power Supply for SLIC



SLIC Inverting-Boost

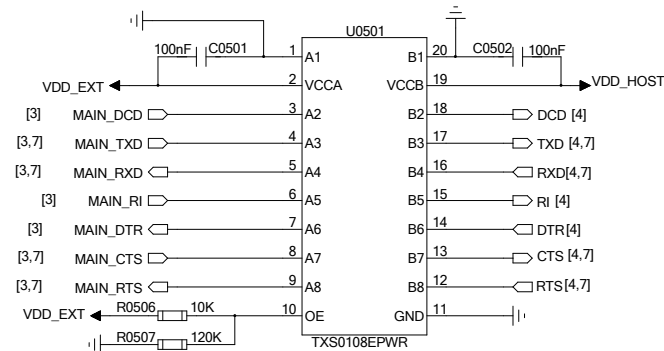


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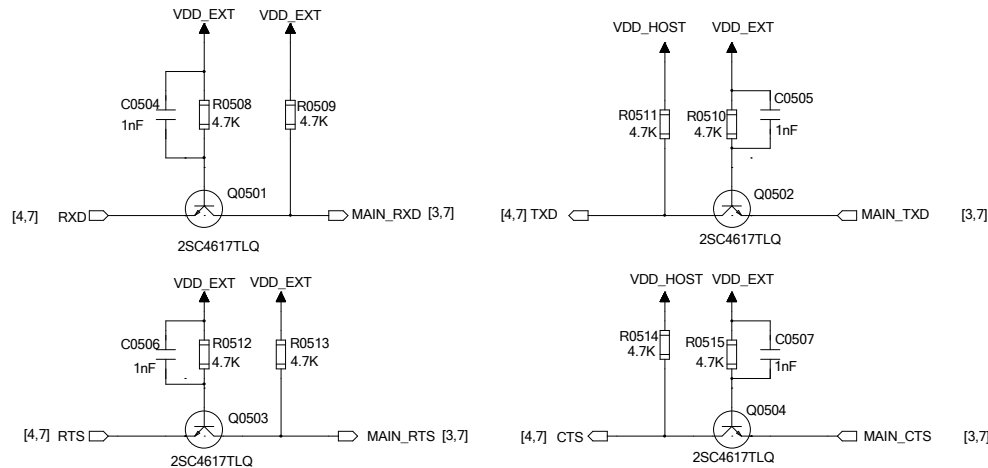
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(U)SIM and UART Designs

UART Level-shifting Circuit - IC Solution (Recommended)



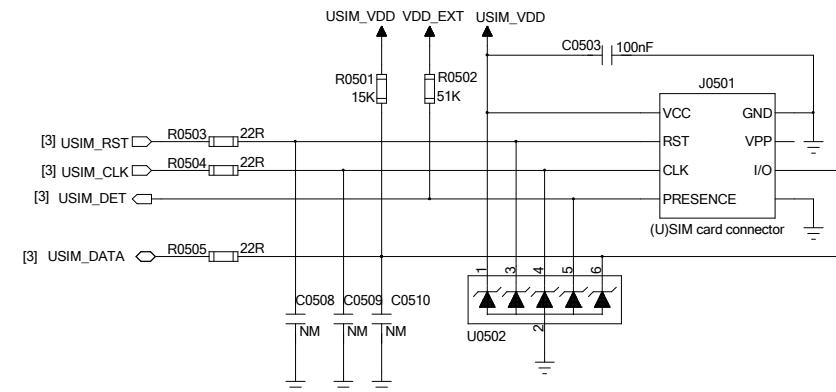
UART Level-shifting Circuit - Transistor Solution



NOTE:

- It is recommended to use an IC conversion chip for UART level-shifting circuit. Transistor solution is not suitable for applications with high baud rates exceeding 460 kbps.
- The voltage supplied to VCCA should not exceed that of VCCB. For more information about TXS0108EPWR, see the datasheet from Texas Instruments.
- If a high baud rate is enabled, it is highly recommended to install four capacitors of 1 nF (C0504/C0505/C0506/C0507) for transistor solutions.
- The transistor solutions of MAIN_DTR is similar to that of MAIN_RTS, and the transistor solutions of and MAIN_RI and MAIN_DCD are similar to that of MAIN_CTS.

(U)SIM Interface



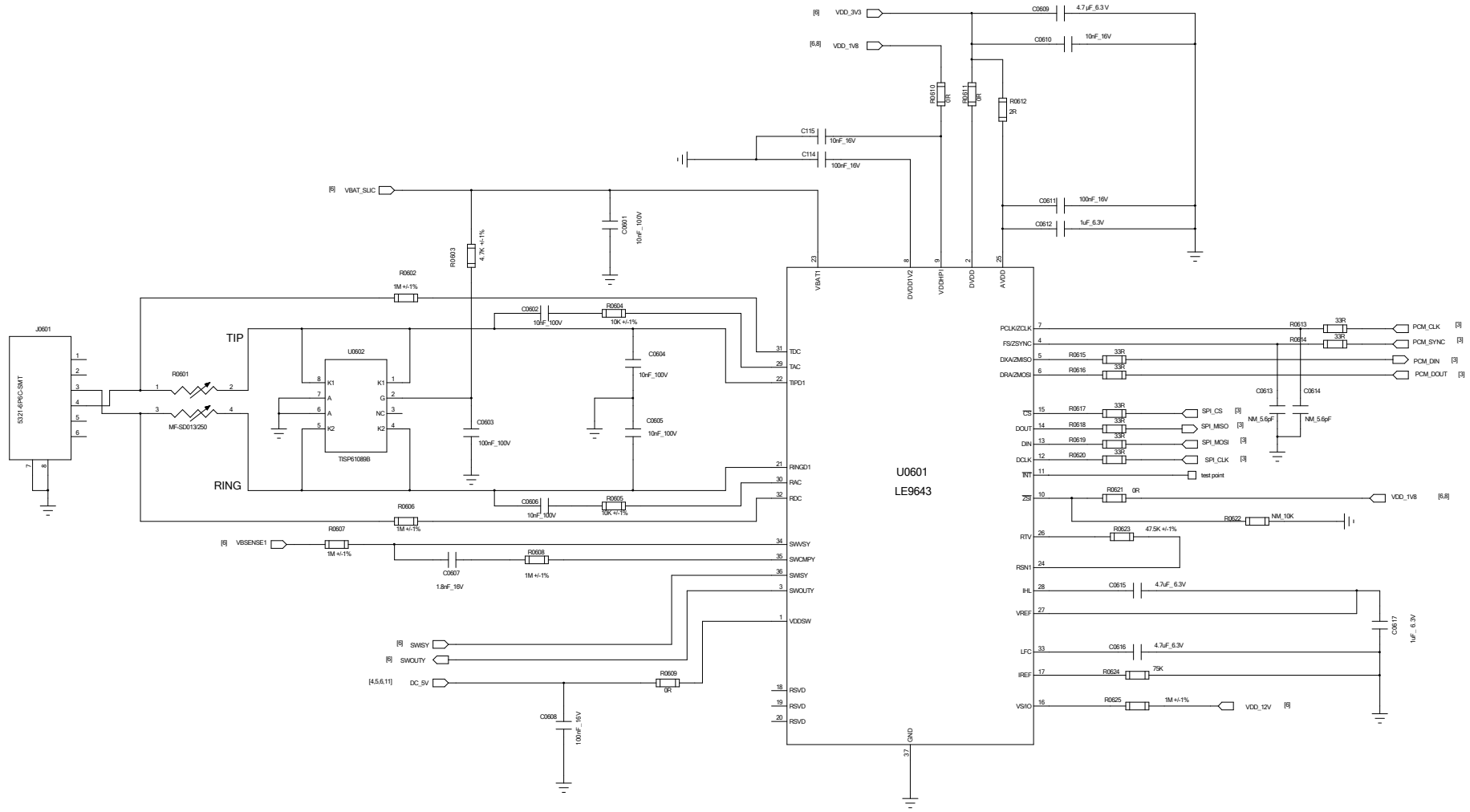
NOTE:

- The module provides two (U)SIM interfaces. The two interfaces have the same design requirements.
- The decoupling capacitor of USIM_VDD should be less than 1 μ F and must be placed close to the (U)SIM card connector.
- The module provides USIM1_DET and USIM2_DET to detect the (U)SIM card. USIM_DET supports both low level and high level detections. For more details, see the *Quectel_EG060K&EG120K_Series_Hardware_Design*.
- R0503-R0505 are applied to suppress the EMI and enhance the ESD protection.
- Please add an ESD component near the (U)SIM card connector. The TVS array with junction capacitance less than 50 pF must be placed as close as possible to the (U)SIM card connector.
- R0501 can improve anti-jamming capability of the (U)SIM circuit and it should be placed near the (U)SIM card connector.
- The bypass capacitors C0508-C0510 are not mounted by default.

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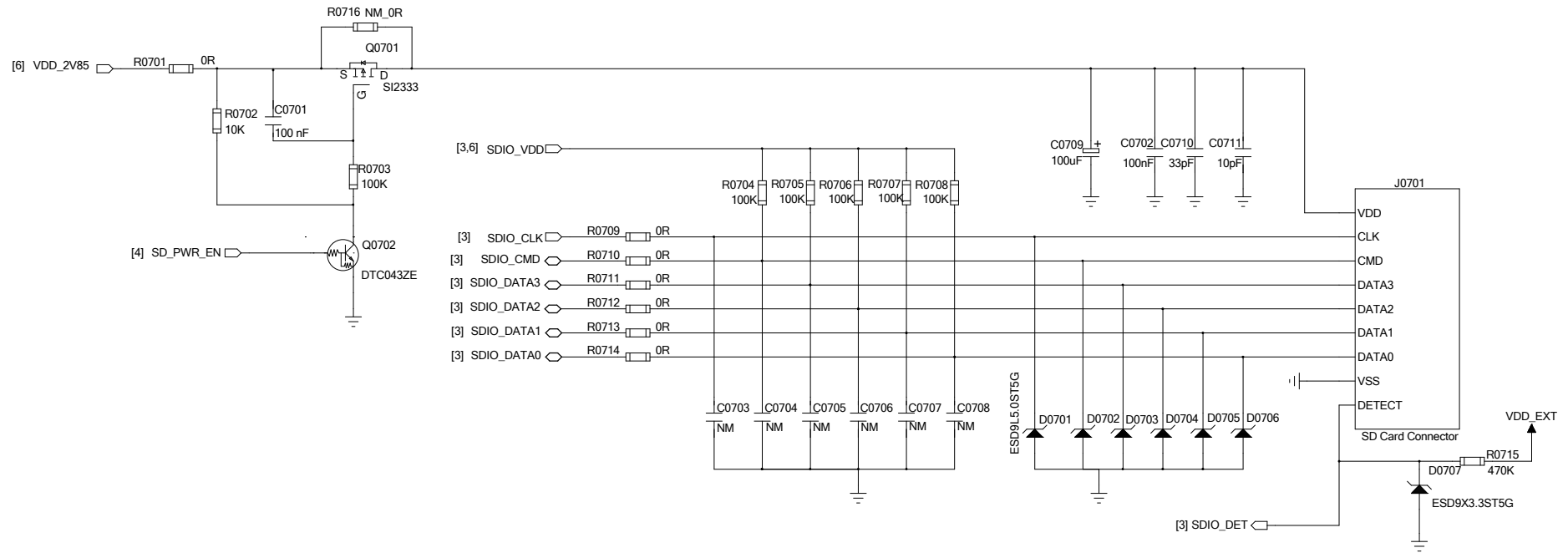
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SLIC Design



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SD Card Design



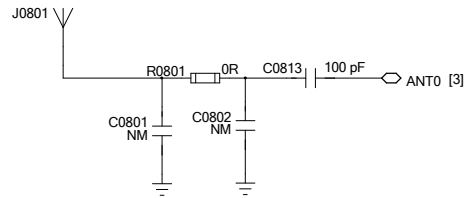
NOTE:

- SDIO_VDD, with a maximum output current of 50 mA, can only be used to supply power for SDIO pull-up resistors.
- The voltage range of SD card power supply is 2.7-3.6 V and a sufficient current up to 0.8 A should be provided.
- To avoid the jitter, resistors R0704-R0708 are needed to pull up the SDIO signals to SDIO_VDD. The value of these resistors is between 10 -100 kΩ and the recommended value is 100 kΩ.
- To improve signal quality, it is recommended to add resistors R0709-R0714 of 0 Ω in series between the module and the SD card connector.
The bypass capacitors C0703-C0708 are not mounted by default. All resistors and bypass capacitors should be close to the module.
- It is recommended to add ESD components near the signal traces.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock signals and DC-DC signals.
- Route SDIO signal traces with 50 Ω impedance. It is important to route SDIO signal traces with total grounding.
- Make sure the adjacent trace spacing is twice the trace width and the bus capacitance is less than 15 pF.
- It is recommended to keep the trace length difference between SDIO_CLK and SDIO_DATA/SDIO_CMD within 1 mm and the total routing length less than 50 mm.
The trace inside the module is 25 mm long in total, so the exterior trace should be less than 25 mm long in total.
- DETECT is an active low pin of an SD card connector, and it must be connected to the module when an SD card is used.

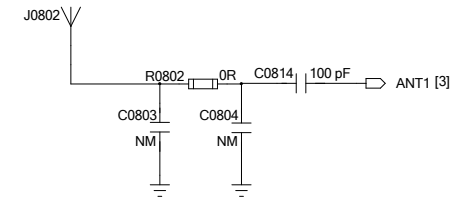
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Antenna Interfaces Design

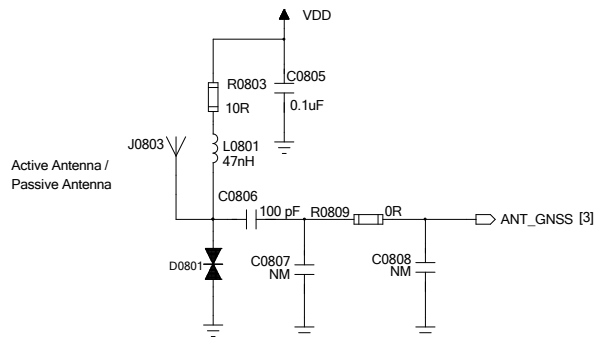
Main Antenna Interface



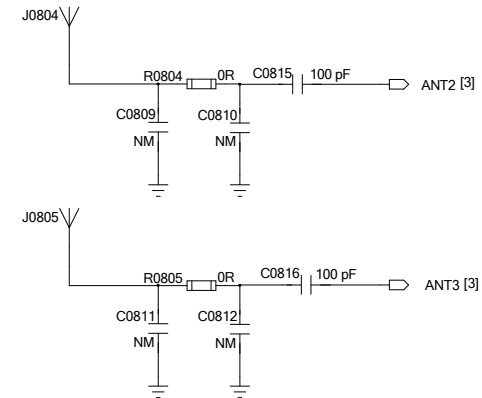
Diversity Antenna Interface



GNSS Antenna Interface



MIMO Antenna Interfaces



NOTE:

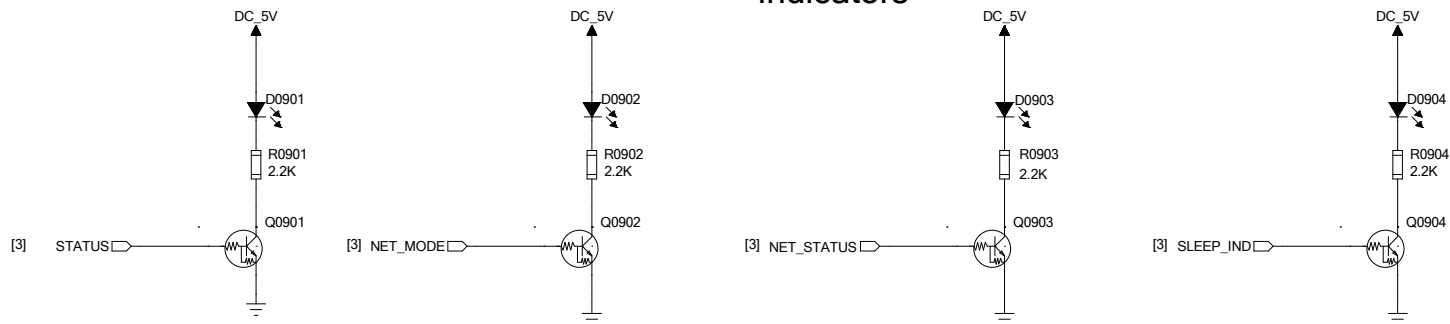
1. A n type circuit is recommended to be used for the module's antenna interfaces to facilitate future debugging.
2. The diversity reception function is ON by default.
3. An external LDO can be used in an active antenna circuit to supply power.
4. If a passive antenna is used in the antenna circuit design, then C0805, D0801, R0803 and L0801 are not needed.
5. ESD protection devices should be added to the GNSS antenna interface, and their parasitic capacitance should be less than 0.05 pF.
6. The impedance of the RF signal traces should remain at 50 Ω when routing.
7. C0813/C0814/C0815/C0816 are DC blocking capacitors. If there is DC power at the antenna ports, the capacitance must be used for DC blocked, and the value can be adjusted according to the actual debugging.

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Indicators and Test Points

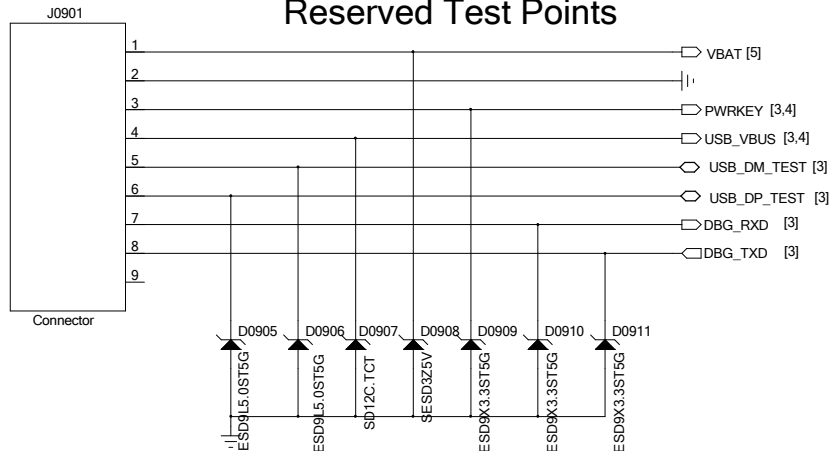
Indicators



NOTE:

1. STATUS is an output pin, and its drive current is less than 1 mA.
2. For more details about NET_MODE and NET_STATUS, see *Quectel_EG060K&EG120K_Series_Hardware_Design*.
3. If the power consumption is required to be as low as possible when the device is in sleep mode, replace the power supply of indicators with a controllable one. Turn off the power supply of the indicators when the module enters sleep mode.

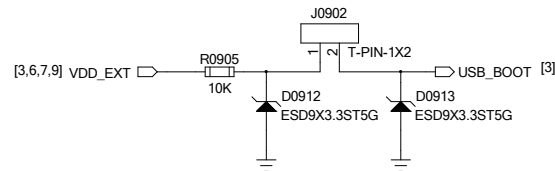
Reserved Test Points



NOTE:

1. Both USB and debug UART interfaces are reserved for software debugging.
2. The USB interface can also be used to upgrade the firmware.
3. Keep USB test points as close to USB pins as possible. Note that the junction capacitance of ESD components on USB data traces might affect the signal quality. Thus, the capacitance should be less than 2 pF.
4. Debug UART interface supports 1.8 V power domain. A voltage-level translator should be used if the power domain of your applications is 3.3 V.

Forced Download Mode



NOTE:

You can pull up USB_BOOT to VDD_EXT before turning on the module, then the module will enter forced download mode when turned on.

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