EG060K&EG120K Series
Hardware Design

LTE-A Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for your failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-01-28	Elliot CAO/ Lewis PENG/ Jacen HUANG	Creation of the document
1.0	2022-03-15	Elliot CAO/ Lewis PENG/ Jacen HUANG	Released
1.1	2023-03-16	Frank GAO/ Lewis PENG/ Jacen HUANG	1. Added EG060K-NA, EG060K-LA, EG120K-NA, EG120K-LA and the relevant information. 2. Added 4 × 4 MIMO frequency band information of EG060K-EA (Table 2). 3. Added B42, B43 and their optional features of EG120K-EA and EG060K-EA (Table 2, Table 32, Table 34, Table 46 and Table 47). 4. Updated the supported USB serial drivers (Table 3). 5. Updated the typical values of GNSS performance (Table 42). 6. Updated the reference design into passive antenna reference design and active antenna reference design (Chapter 5.2.3 and 5.2.4). 7. Updated the GNSS antenna VSWR and added the recommended information about passive GNSS antenna using (Table 43). 8. Changed the minimum and maximum voltage of absolute maximum ratings at ADC (Table 44).

	9. Updated the recommended reflow soldering thermal profile and relevant parameters (Chapter 8.2). 10. Updated the packaging specification (Chapter 8.3).

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Table Index

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1 Introduction

This document defines EG060K and EG120K series modules and describes their air and hardware interfaces which are connected to your applications.

With this document, you can quickly understand module interfaces, electrical and mechanical specifications, as well as other related information of the modules. The document, coupled with application notes and user guides, makes it easy to design and sets up mobile applications with the modules.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA [0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

The module is an LTE/WCDMA wireless communication module with receiving diversity. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA networks.

The module supports embedded operating systems such as Windows, Linux and Android. It also provides GNSS and voice functionality [1] to meet specific application demands.

2.1. Frequency Bands and Functions

The following table shows the frequency bands and GNSS systems supported by the module. For details about CA combinations, see ***documents [1]*** and ***[2]***.

Table 2: Frequency Bands and GNSS Types

Mode	EG060K-EA [2]	EG120K-EA	EG060K-NA	EG120K-NA	EG060K-LA	EG120K-LA
LTE-FDD (with Rx-diversity)	B1/B3/B5/B7/ B8/B20/B28/ B32 [3]	B1/B3/B5/B7/ B8/B20/B28/ B32 [3]	B2/B4/B5/B7/ B12/B13/B14/ B25/B26/B29 [3]/ B30/ B66/B71	B2/B4/B5/B7/B 12/B13/B14/B2 5/B26/ B29 [3]/ B30/ B66/B71	B2/B4/B5/B7/ B8/B25/B28/ B66	B2/B4/B5/B7/ B8/B25/B28/ B66
LTE-TDD (with Rx-diversity)	B38/B40/B41/ B42 [4]/B43 [4]	B38/B40/B41/ B42 [4]/B43 [4]	B41/B48	B41/B48	B42 [4]/B43 [4]	B42 [4]/B43 [4]
LTE DL 4 × 4 MIMO (with Rx-diversity)	B1/B3/B7/B38/ B40/B41/B42 [4]	B1/B3/B7/B38/ B40/B41/B42 [4]	B2/B4/B7/B25/ B30/B41/B48/ B66	B2/B4/B7/B25/ B30/B41/B48/ B66	B2/B4/B7/B25/ B42 [4]/B66	B2/B4/B7/B25/ B42 [4]/B66
WCDMA (with Rx-diversity)	B1/B3/B5/B8	B1/B3/B5/B8	-	-	B2/B4/B5/B8	B2/B4/B5/B8
GNSS	GPS, GLONASS, BDS, Galileo	GPS, GLONASS, BDS, Galileo	GPS, GLONASS, BDS, Galileo	GPS, GLONASS, BDS, Galileo	GPS, GLONASS, BDS, Galileo	GPS, GLONASS, BDS, Galileo

[1] EG060K and EG120K series modules contain **Data + Voice** version and **Data-only** version. **Data + Voice** version supports voice and data functions, while **Data-only** version only supports data function.
[2] For EG060K-EA, bands of LTE DL 4 × 4 MIMO are optional.
[3] LTE-FDD B32, B29 supports Rx only and is only for secondary component carrier.
[4] B42, B43 bands are optional.

With a compact profile of 37.0 mm × 39.5 mm × 2.8 mm, the module meets most of requirements for M2M applications such as industrial routers, home gateways, set-top boxes, industrial PDAs, consumer laptops, rugged tablet PCs, video surveillance and digital signage. The module is an SMD type module and can be embedded in applications through its 299 LGA pins.

2.2. Key Features

Table 3: Key Features

Feature	Details
Power Supply	● Supply voltage range: 3.3–4.4 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 3 (23 dBm ±2 dB) for LTE bands ● Class 3 (23 dBm ±2 dB) for WCDMA bands
LTE Features	● **EG060K-EA** ● Supports 3GPP Rel-12 Cat 6 LTE-FDD and LTE-TDD ● Supports UL QPSK and 16QAM modulations ● Supports DL QPSK, 16QAM and 64QAM modulations ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● LTE-FDD: Max. 300 Mbps (DL)/50 Mbps (UL) ● LTE-TDD: Max. 226 Mbps (DL)/28 Mbps (UL) ● **EG120K-EA** ● Supports 3GPP Rel-12 Cat 12 LTE-FDD and LTE-TDD ● Supports UL QPSK,16QAM and 64QAM modulations ● Supports DL QPSK, 16QAM, 64QAM and 256QAM modulations ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● Supports 4 × 4 MIMO in DL direction ● LTE-FDD: Max. 600 Mbps (DL)/150 Mbps (UL) ● LTE-TDD: Max. 430 Mbps (DL)/90 Mbps (UL) ● **EG060K-NA** ● Supports 3GPP Rel-12 Cat 6 LTE-FDD and LTE-TDD ● Supports UL QPSK and 16QAM modulations ● Supports DL QPSK, 16QAM and 64QAM modulations ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● Supports 4 × 4 MIMO in DL direction ● LTE-FDD: Max. 300 Mbps (DL)/50 Mbps (UL) ● LTE-TDD: Max. 226 Mbps (DL)/28 Mbps (UL) ● **EG120K-NA** ● Supports 3GPP Rel-12 Cat 12 LTE-FDD and LTE-TDD ● Supports UL QPSK,16QAM and 64QAM modulations

	• Supports DL QPSK, 16QAM, 64QAM and 256QAM modulations • Supports 1.4/3/5/10/15/20 MHz RF bandwidths • Supports 4 × 4 MIMO in DL direction • LTE-FDD: Max. 600 Mbps (DL)/150 Mbps (UL) • LTE-TDD: Max. 430 Mbps (DL)/90 Mbps (UL) • **EG060K-LA** • Supports 3GPP Rel-12 Cat 6 LTE-FDD and LTE-TDD • Supports UL QPSK and 16QAM modulations • Supports DL QPSK, 16QAM and 64QAM modulations • Supports 1.4/3/5/10/15/20 MHz RF bandwidths • Supports 4 × 4 MIMO in DL direction • LTE-FDD: Max. 300 Mbps (DL)/50 Mbps (UL) • LTE-TDD: Max. 226 Mbps (DL)/28 Mbps (UL) • **EG120K-LA** • Supports 3GPP Rel-12 Cat 12 LTE-FDD and LTE-TDD • Supports UL QPSK,16QAM and 64QAM modulations • Supports DL QPSK, 16QAM, 64QAM and 256QAM modulations • Supports 1.4/3/5/10/15/20 MHz RF bandwidths • Supports 4 × 4 MIMO in DL direction • LTE-FDD: Max. 600 Mbps (DL)/150 Mbps (UL) • LTE-TDD: Max. 430 Mbps (DL)/90 Mbps (UL)
UMTS Features	• Supports 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA • Supports QPSK, 16QAM and 64QAM modulations • Max. transmission data rates: DC-HSDPA: 42 Mbps (DL) HSUPA: 5.76 Mbps (UL) WCDMA: 384 kbps (DL)/384 kbps (UL)
Internet Protocol Features	Supports QMI/MBIM/NITZ/HTTP/HTTPS/FTP/LwM2M*/PING* protocols
SMS	• Text and PDU modes • Point-to-point MO and MT • SMS cell broadcast • SMS storage: ME by default
(U)SIM Interfaces	• Supports (U)SIM card: 1.8/3.0 V • Supports Dual (U)SIM Single Standby
eSIM	Optional
USB Interface	• Complies with USB 3.0 and 2.0 specifications, with max. transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 • Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output, and voice over USB • Supports USB serial drivers: Windows 7/8/8.1/10/11, Linux 2.6–5.18,

	Android 4.x–12.x
UART Interfaces	**Main UART interface:** ● Used for AT command communication and data transmission ● Baud rate reaches up to 921600 bps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART interface:** ● Used for Linux console and log output ● 115200 bps baud rate **Bluetooth UART interface*:** ● Multiplexed from SPI ● Used for Bluetooth communication ● 115200 bps baud rate
SPI	● Works in master mode only ● Max. clock frequency rate: 50 MHz
Audio Features	● Provides one digital audio interface: PCM interface ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with an external codec or SLIC ● Supports 16-bit linear data format ● Supports long and short frame synchronization ● Supports master and slave modes, but the module must work as master in long frame synchronization
PCIe Interface	● Complies with *PCI Express Base Specification Revision 2.0* ● PCIe × 1, supporting 5 Gbps per lane ● Used for data transmission ● RC mode only ● For WLAN, Ethernet functions
Antenna Interfaces	● ANT [0:3] ● ANT_GNSS ● 50 Ω impedance
Rx-diversity	Supports LTE/WCDMA Rx-diversity
GNSS Features	● Supports GPS, GLONASS, BDS, and Galileo ● Protocol: NMEA 0183 ● Data update rate: 1 Hz
AT Commands	● Complies with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Network Indication	● NET_MODE ● NET_STATUS ● For network connectivity status indication
Physical Characteristics	● Dimensions: (37.0 ±0.2) mm × (39.5 ±0.2) mm × (2.8 ±0.2) mm ● Package: LGA ● Weight: approx. 9.1 g

Temperature Ranges	● Operating temperature range: -30 to +75 °C [5] ● Extended temperature range: -40 to +85 °C [6] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● USB 2.0 interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR2 SDRAM + NAND flash
- Radio frequency
- Peripheral interfaces

[5] To meet this operating temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this operation temperature range, the module can meet 3GPP specifications.

[6] To meet this extended temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this extended temperature range, the module remains the ability to establish and maintain functions like SMS, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

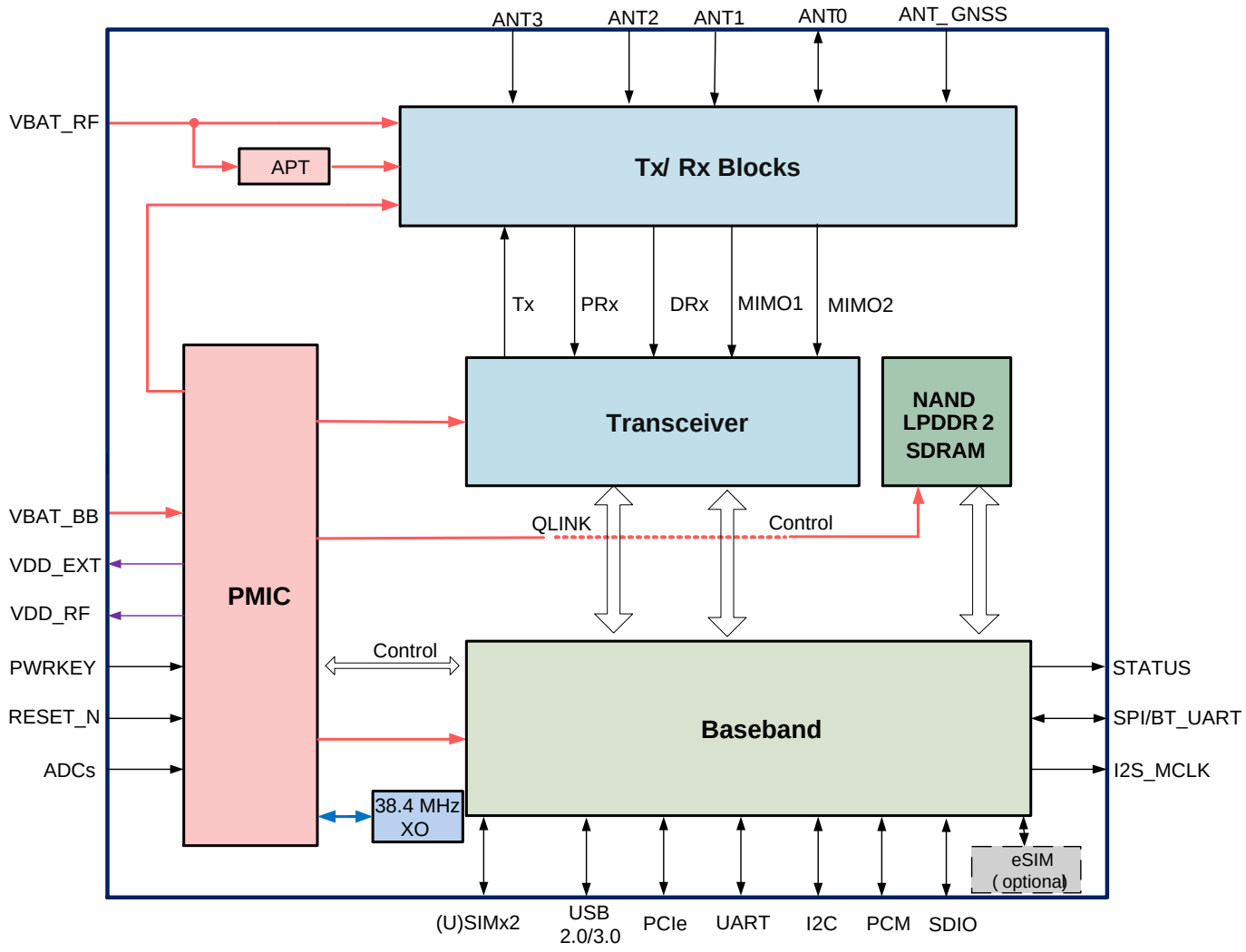


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

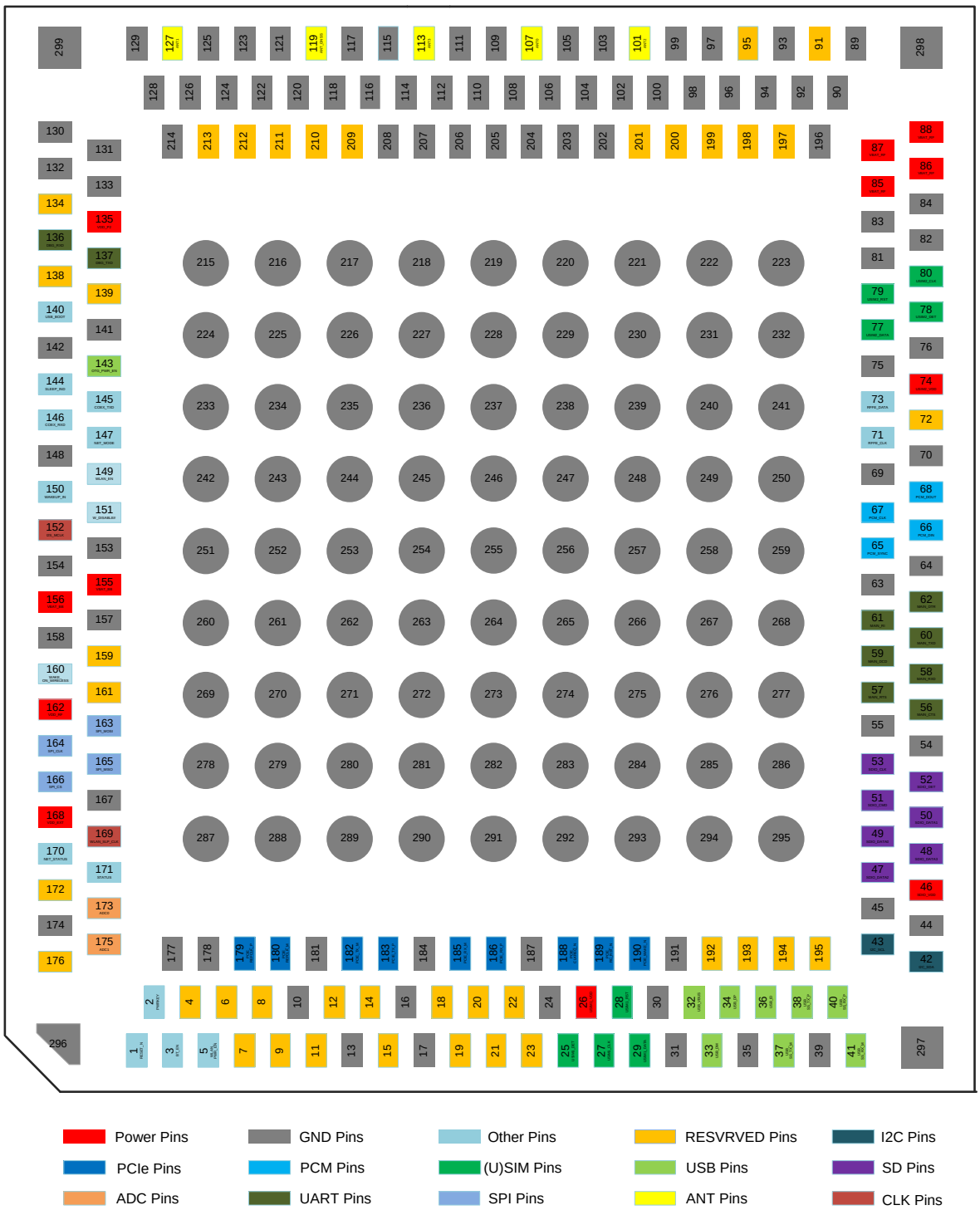


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins and unused pins open.
2. GND pins should be connected to ground in the design.

2.5. Pin Description

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current, etc.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	155, 156	PI	Power supply for the module's baseband part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	Sufficient current up to 1 A is requisite.
VBAT_RF	85–88	PI	Power supply for the module's RF part		A transmitting burst requires a sufficient current up to 1.2 A.
VDD_EXT	168	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	A test point is recommended to be reserved.
VDD_RF	162	PO	Provide 2.85 V for external RF circuit	Vnom = 2.7 V $I_O$max = 120 mA	If unused, keep it open.

GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114–118, 120–126, 128–133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202–208, 214–299

Turn On/Off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESET_N	1	DI	Reset the module	V_{IH}min = 1.17 V V_{IL}max = 0.54 V	Pulled up to 1.8 V internally. Active low. A test point is recommended to be reserved.
PWRKEY	2	DI	Turn on/off the module		Pulled up to 1.8 V internally. Active low.

Status Indication

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
NET_MODE	147	DO	Indicate the module's network registration mode	VDD_EXT	If unused, keep them open.
NET_STATUS	170	DO	Indicate the module's network activity status		
STATUS	171	DO	Indicate the module's operation status		
SLEEP_IND	144	DO	Indicate the module's sleep mode		

(U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_DET	25	DI	(U)SIM1 card hot-swap detect	VDD_EXT	If unused, keep it open.
USIM1_VDD	26	PO	(U)SIM1 card power supply	**High-voltage:** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V	

				Low-Voltage: Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	
USIM1_CLK	27	DO	(U)SIM1 card clock	USIM1_VDD	
USIM1_RST	28	DO	(U)SIM1 card reset		
USIM1_DATA	29	DIO	(U)SIM1 card data		
USIM2_VDD	74	PO	(U)SIM2 card power supply	**High-voltage:** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V **Low-Voltage:** Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	If (U)SIM2 interface is unused, keep it open.
USIM2_DATA	77	DIO	(U)SIM2 card data	USIM2_VDD	If (U)SIM2 interface is unused, keep it open.
USIM2_DET	78	DI	(U)SIM2 card detect	VDD_EXT	If (U)SIM2 interface is unused, keep it open.
USIM2_RST	79	DO	(U)SIM2 card reset	USIM2_VDD	If (U)SIM2 interface is unused, keep them open.
USIM2_CLK	80	DO	(U)SIM2 card clock		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	32	DI	USB connection detect		Detection threshold: Vmin = 3.3 V Vnom = 5 V Vmax = 5.25 V A test point must be reserved.
USB_DM	33	AIO	USB 2.0 differential data (-)		Comply with USB 2.0 specifications. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DP	34	AIO	USB 2.0 differential data (+)		

USB_SS_TX_M	37	AO	USB 3.0 super-speed transmit (-)		Comply with USB 3.0 specifications. Require differential impedance of 90 Ω.
USB_SS_TX_P	38	AO	USB 3.0 super-speed transmit (+)		
USB_SS_RX_P	40	AI	USB 3.0 super-speed receive (+)		
USB_SS_RX_M	41	AI	USB 3.0 super-speed receive (-)		
USB_ID*	36	DI	USB ID detect	VDD_EXT	If unused, keep them open.
OTG_PWR_EN*	143	DO	OTG power control		
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_P2	135	PI	Power input for SDIO interface		If a SD card is used, connect VDD_P2 to SDIO_VDD. If unused, connect VDD_P2 to VDD_EXT.
SDIO_VDD	46	PO	SD card application: SDIO pull up power supply	**High-voltage:** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V **Low-Voltage:** Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	Cannot work as SD card power supply. SD card must be powered by an external power supply.
SDIO_DATA0	49	DIO	SDIO data bit 0	SDIO_VDD	If unused, keep them open.
SDIO_DATA1	50	DIO	SDIO data bit 1		
SDIO_DATA2	47	DIO	SDIO data bit 2		
SDIO_DATA3	48	DIO	SDIO data bit 3		
SDIO_CMD	51	DIO	SDIO command		
SDIO_CLK	53	DO	SDIO clock		
SDIO_DET	52	DI	SD card detect	VDD_EXT	If unused, keep it open.

Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	56	DO	Main UART clear to send	VDD_EXT	CTS: Connect to DTE's CTS If unused, keep it open.
MAIN_RTS	57	DI	Main UART request to send		RTS: Connect to DTE's RTS If unused, keep it open.
MAIN_RXD	58	DI	Main UART receive		If unused, keep them open.
MAIN_DCD	59	DO	Main UART data carrier detect		
MAIN_TXD	60	DO	Main UART transmit		
MAIN_RI	61	DO	Main UART ring indication		
MAIN_DTR	62	DI	Main UART data terminal ready		Pulled up by default. Pulling low will awaken the module. If unused, keep it open. Sleep mode control.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	136	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	137	DO	Debug UART transmit		
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_MOSI	163	DO	SPI master-out slave-in	VDD_EXT	If unused, keep it open. It can be multiplexed into BT_TXD*.
SPI_CLK	164	DO	SPI clock		If unused, keep it open. It can be multiplexed into BT_CTS*.
SPI_MISO	165	DI	SPI master-in slave-out		If unused, keep it open. It can be multiplexed

					into BT_RXD*.
SPI_CS	166	DO	SPI chip select		If unused, keep it open. It can be multiplexed into BT_RTS*.
PCM and I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SDA	42	OD	I2C serial data (for an external codec)	VDD_EXT	An external pull-up resistor is requisite. If unused, keep them open.
I2C_SCL	43	OD	I2C serial clock (for an external codec)		
PCM_SYNC	65	DIO	PCM data frame sync		Output signal in master mode. Input signal in slave mode. If unused, keep it open.
PCM_DIN	66	DI	PCM data input		If unused, keep it open.
PCM_CLK	67	DIO	PCM clock		Output signal in master mode. Input signal in slave mode. If unused, keep it open.
PCM_DOUT	68	DO	PCM data output		If unused, keep it open.
I2S_MCLK	152	DO	Clock output for codec		Provide a digital clock output for an external codec. If unused, keep it open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT0	107	AIO	Main antenna interface		50 Ω impedance
ANT1	127	AI	Rx-diversity antenna interface		50 Ω impedance If unused, keep them open.
ANT2	101	AI	4 × 4 MIMO antenna interface		
ANT3	113	AI			

ANT_GNSS	119	AI	GNSS antenna interface		
WLAN Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_PWR_EN	5	DO	WLAN power supply enable control	VDD_EXT	If unused, keep them open.
COEX_TXD	145	DO	LTE/WLAN coexistence transmit		
COEX_RXD	146	DI	LTE/WLAN coexistence receive		
WLAN_EN	149	DO	WLAN function enable control		Active high. If unused, keep it open.
WAKE_ON_WIRELESS	160	DI	Awaken the host (the module) via an external Wi-Fi module		Active low. If unused, keep it open.
WLAN_SLP_CLK	169	DO	WLAN sleep clock		If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	173	AI	General-purpose ADC interface	0–1.875 V	If unused, keep them open.
ADC1	175	AI			
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	179	AO	PCIe reference clock (+)		Require differential impedance of 95 Ω. If unused, keep them open. Require differential impedance of 95 Ω.
PCIE_REFCLK_M	180	AO	PCIe reference clock (-)		
PCIE_TX_M	182	AO	PCIe transmit (-)		
PCIE_TX_P	183	AO	PCIe transmit (+)		
PCIE_RX_M	185	AI	PCIe receive (-)		

PCIE_RX_P	186	AI	PCIe receive (+)		
PCIE_CLKREQ_N	188	DI	PCIe clock request	VDD_EXT	Input signal in master mode. If unused, keep it open.
PCIE_RC_RST_N	189	DO	PCIe RC reset		Output signal in master mode. If unused, keep it open.
PCIE_WAKE_N	190	DI	PCIe awake		Input signal, in master mode only. If unused, keep it open.
Antenna Tuner Control Interfaces* (RFFE Interface)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RFFE_CLK	71	DO	Used for external MIPI IC control	VDD_EXT	If unused, keep them open.
RFFE_DATA	73	DIO	Used for external MIPI IC control		
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	140	DI	Force the module into emergency download mode	VDD_EXT	Active high. A test point is recommended to be reserved.
BT_EN*	3	DO	Bluetooth function enable control		If unused, keep it open.
WAKEUP_IN	150	DI	Wake up the module		Pulled up by default. Low level awakens the module. If unused, keep it open.
W_DISABLE#	151	DI	Airplane mode control		Pulled up by default. In low level, the module will enter airplane mode. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	4, 6–9, 11, 12, 14, 15, 18–23, 72, 91, 95, 134, 138, 139, 159, 161, 172, 176, 192–195, 197–201, 209–213				Keep these pins open.

2.6. EVB Kit

To help you develop applications conveniently with the module, Quectel supplies an evaluation board (UMTS & LTE EVB R2.0) with accessories to control or test the module. For more details, see ***document [3]***.

3 Operating Characteristics

3.1. Operating Modes

Table 6: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice/Data	Network is connected. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** sets the module to minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or driving W_DISABLE# low will set the module to airplane mode. In this case, the RF function is invalid.	
Sleep Mode	When **AT+QSCLK=1** is executed and the host's USB bus enters suspend state, the module will enter sleep mode. The module keeps receiving paging messages, SMS, voice call and TCP/UDP data from the network with its current consumption reducing to the minimal level.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is inactive, all application interfaces are inaccessible, and the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

See ***document [4]*** for details about **AT+CFUN=0**, **AT+CFUN=4** and **AT+QSCLK=1**.

3.1.1. Sleep Mode

DRX can reduce the current power consumption of the module to the minimum value during sleep mode, and DRX cycle index values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the current power consumption in sleep mode. The longer the DRX cycle is, the lower the power consumption will be.

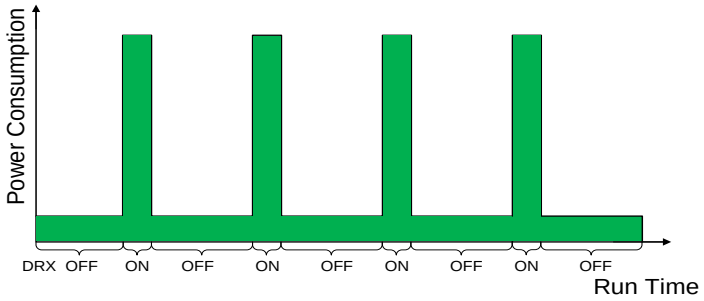


Figure 3: DRX Run Time and Power Consumption in Sleep Mode

The following part of this section presents the power saving procedure and sleep mode of the module.

3.1.1.1.UART Application

If the host communicates with the module via UART interfaces, the following two conditions must be met simultaneously to bring the module into sleep mode.

- Execute **AT+QSCLK=1**.
- Drive MAIN_DTR high.

The following figure shows the connection between the module and the host.

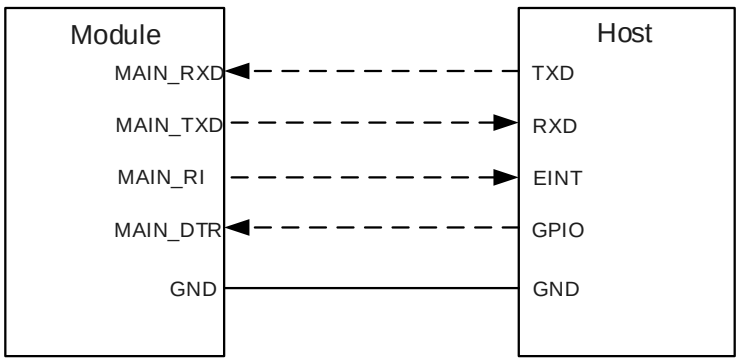


Figure 4: Sleep Mode Application via UART Interfaces

Driving MAIN_DTR low will wake up the module. When the module has a URC to report, MAIN_RI signal will wake up the host. See ***Chapter 4.8*** for details about MAIN_RI behavior.

3.1.1.2.USB Application

USB application can be applied with USB remote wake-up function or USB suspend/resume and RI functions.

If the host supports USB suspend/resume and remote wake-up function, meeting the following three requirements will bring the module into sleep mode.

- Execute **AT+QSCLK=1**.
- Keep MAIN_DTR high (pulled up by default).
- The host's USB bus, connected to the module's USB interface, has entered suspend state.

The following figure shows the above-mentioned connection between the module and the host.

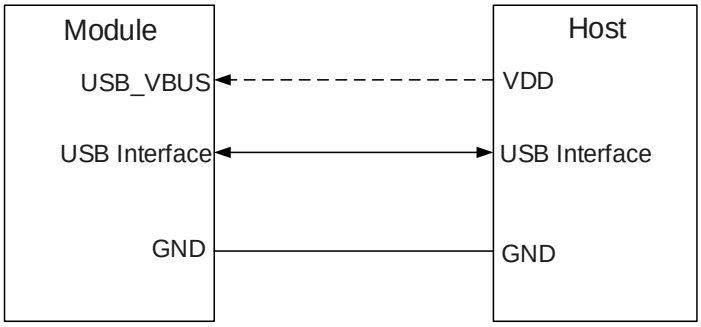


Figure 5: Sleep Mode Application with USB Remote Wake-up

Sending data to the module through USB will wake up the module. When the module has a URC to report, the module will send remote wake-up signals via USB bus to awaken the host.

If the host supports USB suspend/resume but does not support remote wake-up function, meeting the following three requirements will bring the module into sleep mode.

- Execute **AT+QSCLK=1**.
- Keep MAIN_DTR high (pulled up by default).
- The host's USB bus, connected with the module's USB interface, has entered suspend state.

The following figure shows the connection between the module and the host.

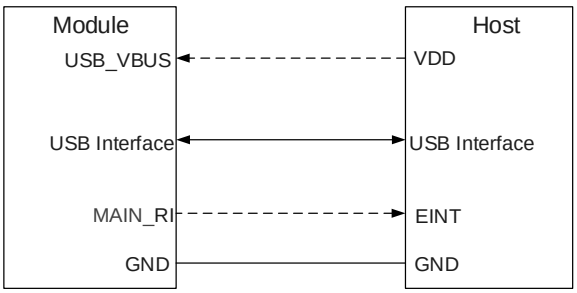


Figure 6: Sleep Mode Application with Suspend function

Sending data to the module through USB will awaken the module. When the module has a URC to report, MAIN_RI will wake up the host.

If the host does not support USB suspend function, USB_VBUS should be disconnected with an external control circuit to bring the module into sleep mode.

- Execute **AT+QSCLK=1**.
- Keep MAIN_DTR high (pulled up by default).
- Disconnect USB_VBUS.

The following figure shows the above-mentioned connection between the module and the host.

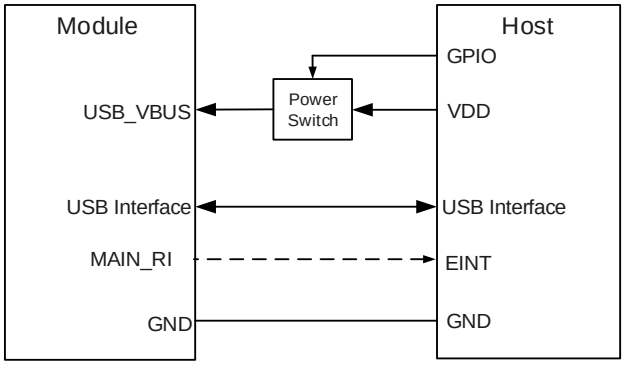


Figure 7: Sleep Mode Application without Suspend Function

To awaken the module, power USB_VBUS by turning on the power switch.

NOTE

Pay attention to the level match shown in dotted line between the module and the host.

3.1.2. Airplane Mode

The module provides W_DISABLE# to disable or enable airplane mode via hardware operation. W_DISABLE# is pulled up by default. Driving it low will bring the module into airplane mode.

Table 7: Pin Description of W_DISABLE#

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	151	DI	Airplane mode control	Pulled up by default. In low level, the module will enter airplane mode. If unused, keep it open.

In airplane mode, the RF function is disabled by default, but it can also be enabled or disabled through AT commands. The following table shows the RF function status of the module.

Table 8: RF Function Status

W_DISABLE# Logic Level	AT Command	RF Function Status	Operating Modes
High Level	**AT+CFUN=1**	Enable	Full functionality mode
	AT+CFUN=0	Disable	Minimum functionality mode
	AT+CFUN=4	Disable	Airplane mode
Low Level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disable	Airplane mode

NOTE

1. W_DISABLE# for airplane mode control function is disabled by default.
2. The execution of **AT+CFUN** will not affect GNSS function.
3. See ***document [4]*** for details about related AT commands mentioned in the above table.

3.2. Power Supply

3.2.1. Power Supply Pins

The module provides six VBAT pins dedicated to the connection to an external power supply. There are two separate voltage domains for VBAT.

- Four VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part.

The following table shows details of VBAT pins and ground pins.

Table 9: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85–88	PI	Power supply for the module's RF part	3.3	3.8	4.4	V
VBAT_BB	155, 156	PI	Power supply for the module's baseband part	3.3	3.8	4.4	V
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114–118, 120–126, 128-133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202–208, 214–299						

The power supply of the module ranges from 3.3 V to 4.4 V. Make sure the input voltage never drops below 3.3 V, otherwise the module will be turned off automatically. The following figure shows the voltage drop during Tx power in 3G/4G networks.

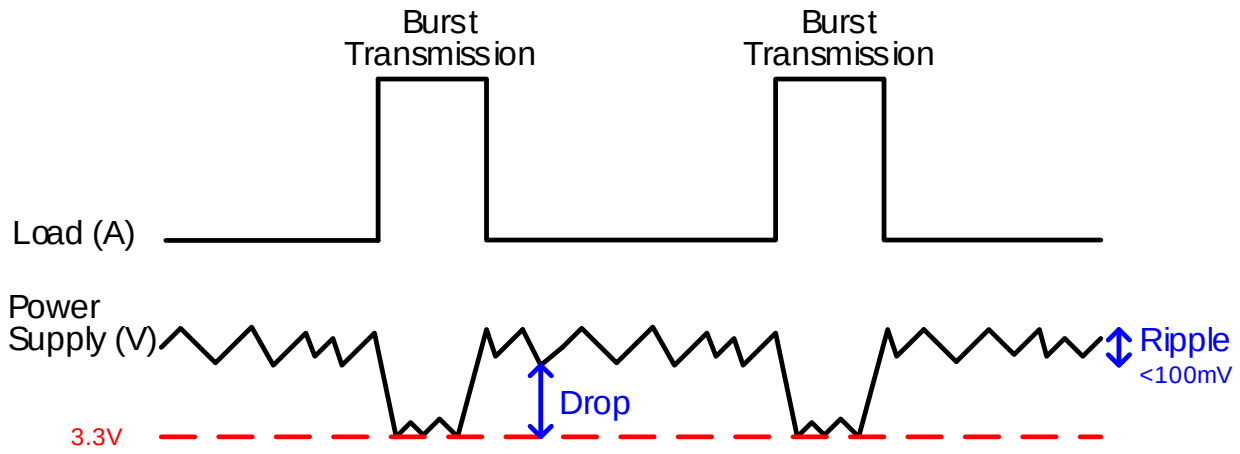


Figure 8: Power Supply Limits during Burst Transmission

To decrease voltage's drop, one bypass capacitor of about 100 μF with low ESR should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to their ultra-low ESR. It is recommended to adopt ceramic capacitors for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source which can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be not less than 2 mm, and the width of VBAT_RF should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, for stable power supply, it is necessary to add a high-power TVS near VBAT_BB and VBAT_RF. The star structure of the power supply is shown below.

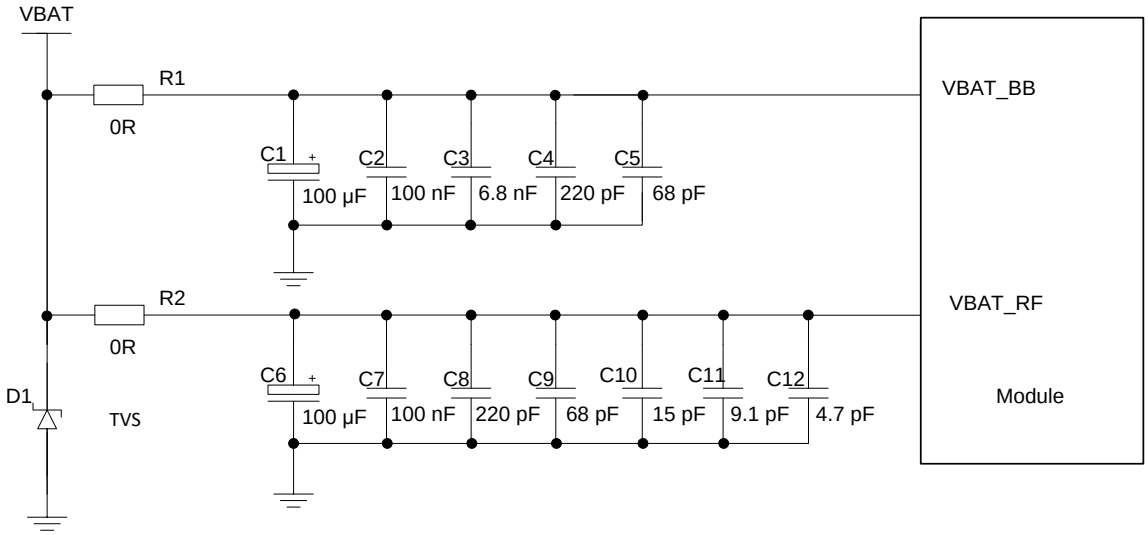


Figure 9: Star Structure of the Power Supply

3.2.2. Reference Design for Power Supply

The performance of the module largely depends on the power supply design. The continuous current of the power supply should be no more than 2 A and the peak current should be no more than 3 A. If the voltage drop between the input and output is not too high, powering the module with an LDO is recommended. If a big voltage difference exists between the input and the desired output (VBAT), a buck DC-DC converter is preferred.

The following figure shows a reference design for +5 V input power source. In this design, the typical power supply output is about 3.8 V.

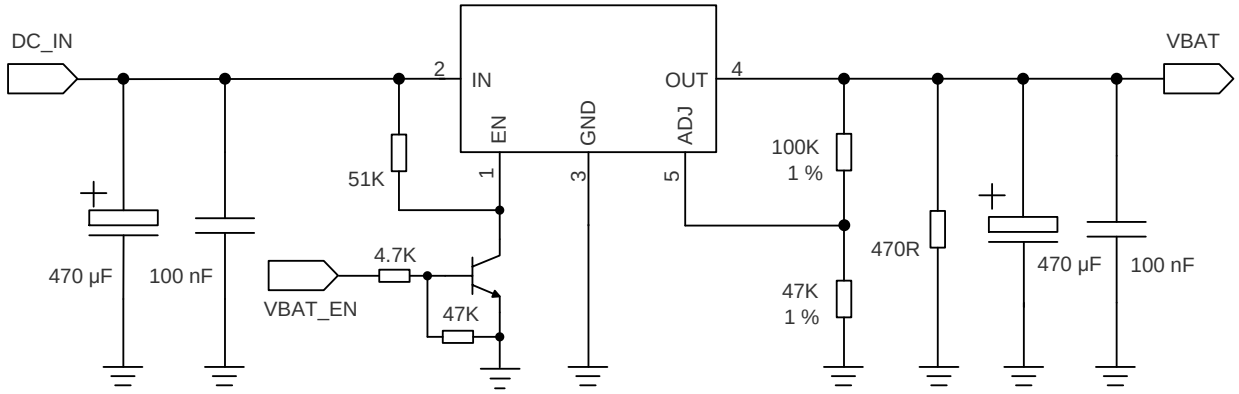


Figure 10: Reference Circuit of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.

3.2.3. Power Supply Voltage Monitoring

AT+CBC can monitor the VBAT_BB voltage value. See ***document [4]*** for details.

3.3. Turn On

The module can be turned on via PWRKEY.

Table 10: PWRKEY Pin Description

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	2	DI	Turn on/off the module	Pulled-up internally. Active low.

When the module is in turn-off mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to control PWRKEY with an open drain/collector driver. After STATUS outputs a high level, PWRKEY can be released. A simple reference circuit is given below.

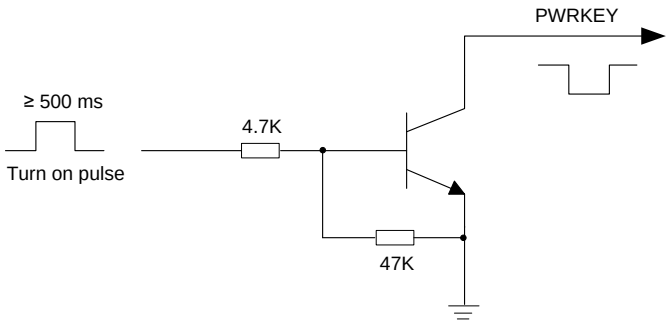


Figure 11: Turn On the Module with a Driving Circuit

Another way to control the PWRKEY is using a button directly. When you are pressing the key, electrostatic strike may be generated from finger. Therefore, it is necessary to place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

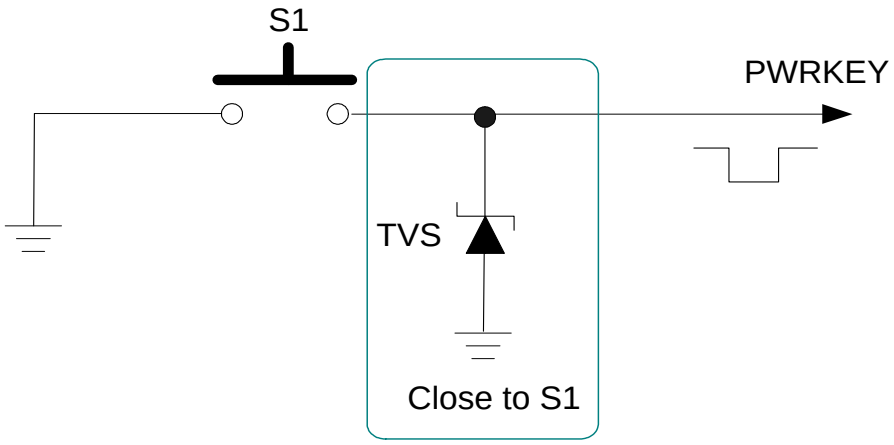


Figure 12: Turn On the Module With a Button

The turn-on timing is illustrated in the following figure.

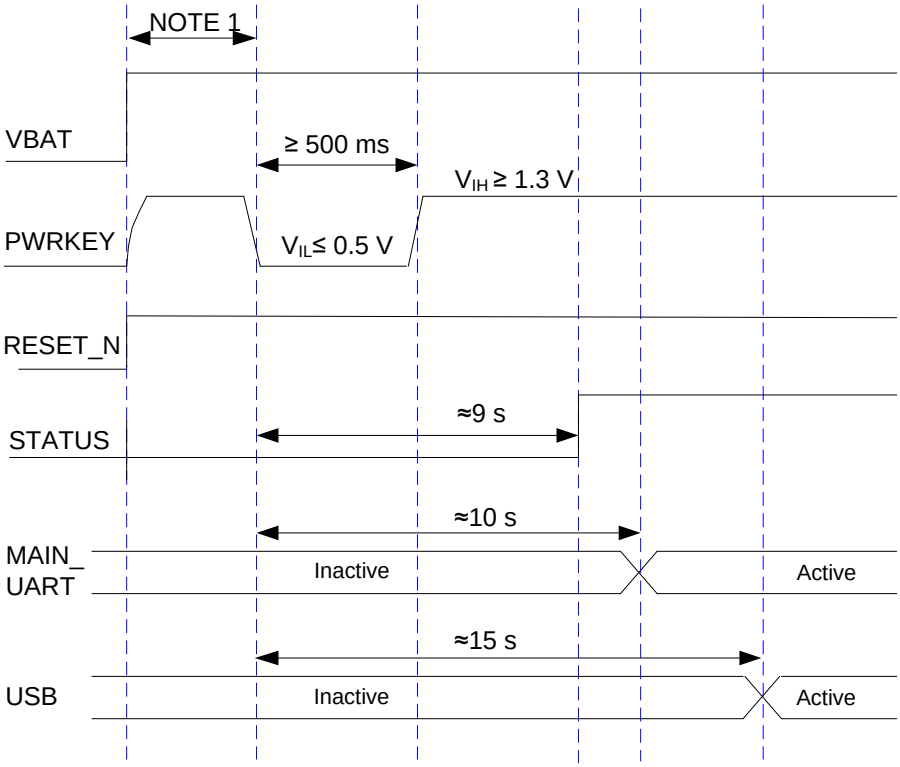


Figure 13: Power-up Timing

NOTE

1. Make sure VBAT has been stable for over 30 ms before pulling down PWRKEY pin.
2. If the module needs to be turned on automatically and turn-off is not needed, PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor.
3. Make sure there is no large capacitance on PWRKEY and RESET_N pins.

3.4. Turn Off

The module can be turned off normally via two methods: using PWRKEY or executing **AT+QPOWD**. See ***document [4]*** for details about the AT command.

3.4.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 800 ms, the module will execute the power-down procedure after PWRKEY is released. The turn-off timing is illustrated in the following figure.

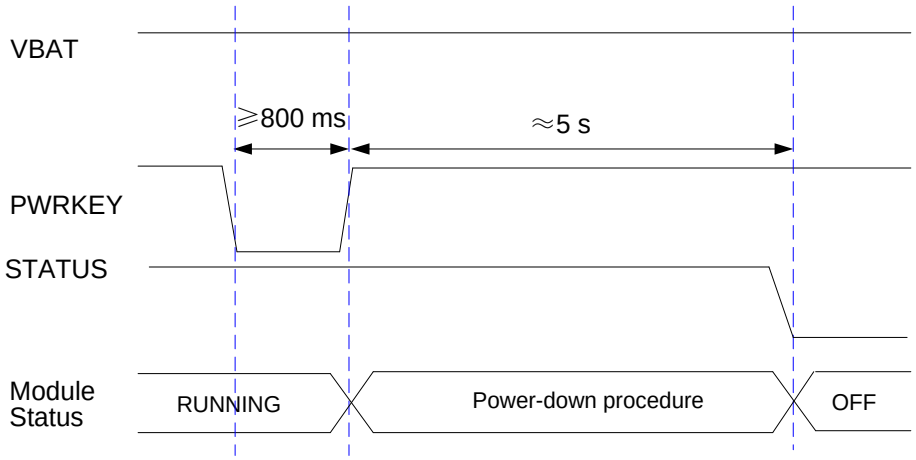


Figure 14: Power-down Timing

3.4.2. Turn Off with AT Command

It is also a safe manner to turn off the module via **AT+QPOWD**. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise the module will be turned on again after a successfully turn-off. See ***document [4]*** for details about the AT command.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise the module will be turned on again after successfully turn-off.

3.5. Reset

The module can be reset by driving RESET_N low for 250-600 ms and then releasing it.

Table 11: RESET_N Pin Description

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	1	DI	Reset the module	Pulled up internally. Active low. A test point is recommended to be reserved.

The recommended circuit is similar to the PWRKEY control circuit. You can use an open drain/collector driver or button to control RESET_N.

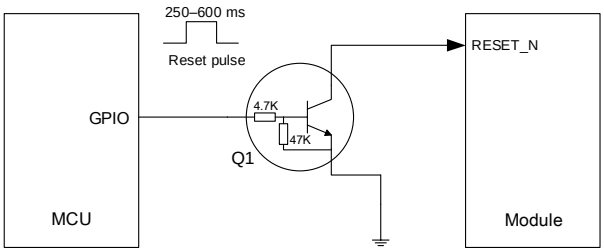


Figure 15: Reference Circuit of RESET_N with a Driving Circuit

The reset timing is illustrated in the following figure.

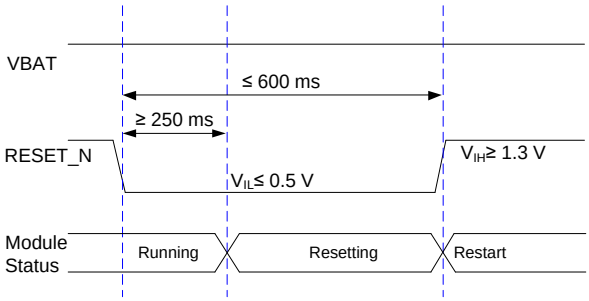


Figure 16: Reset Timing

NOTE

1. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

4 Application Interfaces

The module is designed with 299 LGA pins that can be connected to cellular application platform. This chapter mainly describes the following application interfaces and indication signals of the module:

- (U)SIM interfaces
- USB interface
- UART interfaces
- SPI [7]
- PCM and I2C interfaces
- ADC interfaces
- Network status indication
- Module status indication
- RI
- PCIe interface
- SDIO interface
- Antenna tuner control interfaces*
- USB_BOOT interface

[7] SPI can be multiplexed as Bluetooth UART interface*.

4.1. (U)SIM Interfaces

The module provides two (U)SIM interfaces. The circuitry of (U)SIM interfaces meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported, and Dual SIM Single Standby function is supported. (U)SIM card hot-swap is enabled by **AT+QUIMSLOT**. See ***document [4]*** for details about the AT command.

Table 12: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	25	DI	USIM1 card hot-swap detect	If unused, keep it open.
USIM1_VDD	26	PO	USIM1 card power supply	
USIM1_CLK	27	DO	USIM1 card clock	
USIM1_RST	28	DO	USIM1 card reset	
USIM1_DATA	29	DIO	USIM1 card data	
USIM2_VDD	74	PO	USIM2 card power supply	If USIM2 interface is unused, keep it open.
USIM2_DATA	77	DIO	USIM2 card data	If USIM2 interface is unused, keep it open.
USIM2_DET	78	DI	USIM2 card hot-swap detect	If USIM2 interface is unused, keep it open.
USIM2_RST	79	DO	USIM2 card reset	If USIM2 interface is unused, keep them open.
USIM2_CLK	80	DO	USIM2 card clock	

The module supports (U)SIM card hot-swap via USIM_DET pins, and both high and low level detection are supported. The function is disabled by default, and see **AT+QSIMDET** in ***document [4]*** for more details.

The following figure shows a reference design for (U)SIM interfaces with an 8-pin (U)SIM card connector.

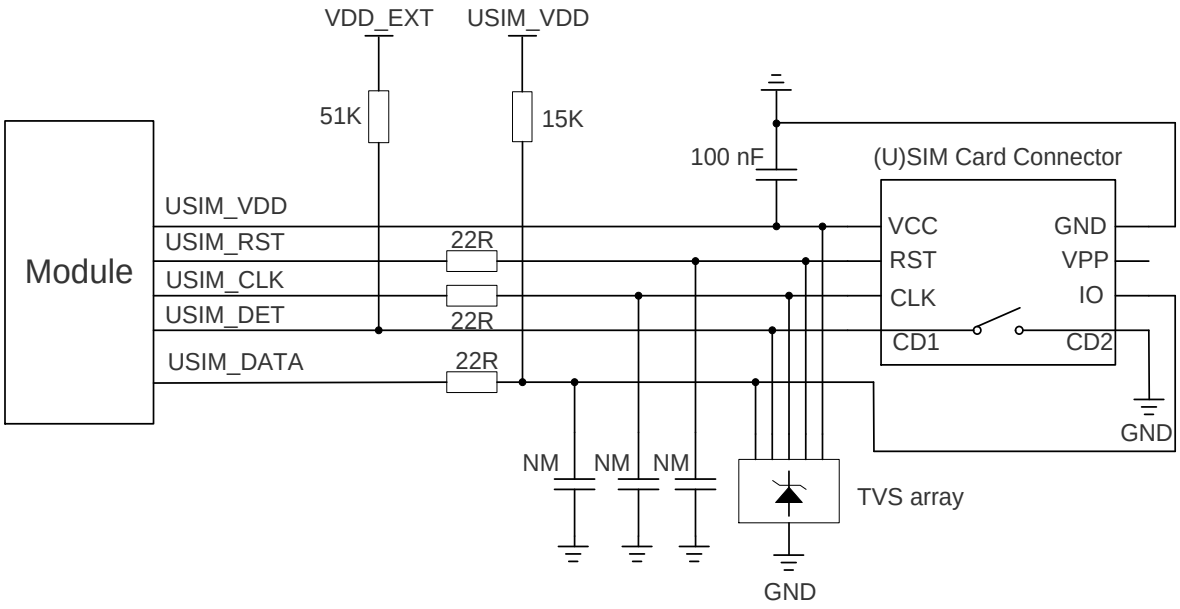


Figure 17: Reference Circuit of (U)SIM Interfaces with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is unnecessary, keep USIM_DET open. A reference circuit for (U)SIM interfaces with a 6-pin (U)SIM card connector is illustrated in the following figure.

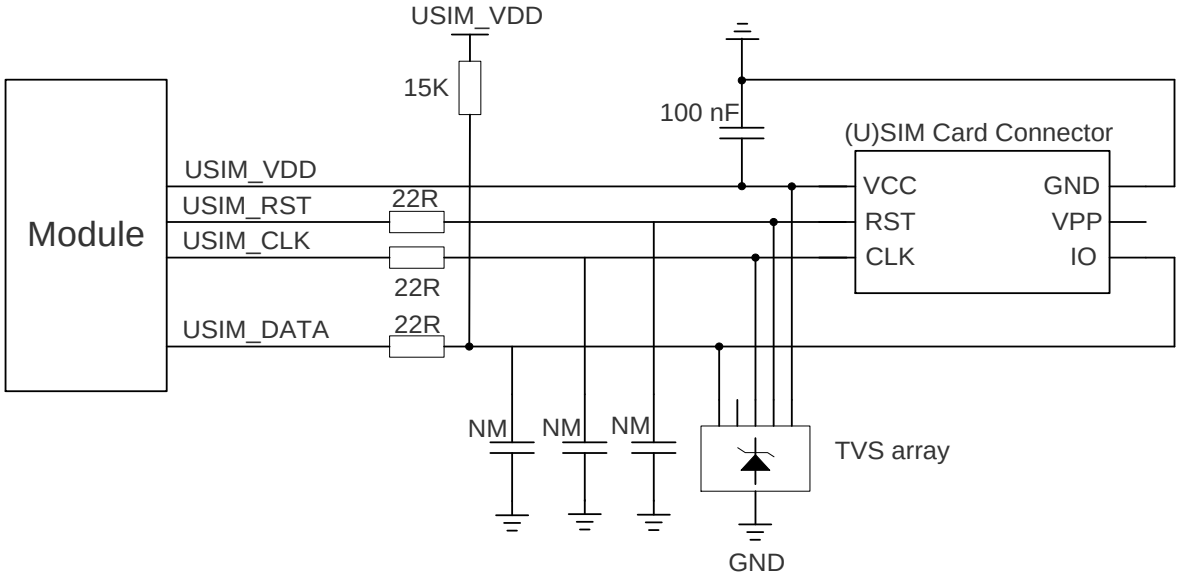


Figure 18: Reference Circuit of (U)SIM Interfaces with a 6-Pin (U)SIM Card Connector

For better reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Put the (U)SIM card connector as close as possible to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make sure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- For better ESD protection, it is recommended to add an ESD protection component of which parasitic capacitance should be less than 50 pF. 22 Ω resistors should be added in series between the module and the (U)SIM card connector to facilitate debugging. The (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability with the application of long layout trace and sensitive occasions, and it should be close to the (U)SIM card connector.

4.2. USB Interface

The module provides one integrated USB (Universal Serial Bus) interface which complies with the USB 3.0 and 2.0 specifications and supports SuperSpeed (5 Gbps) mode on USB 3.0 and high-speed (480 Mbps) and full-speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade, and voice over USB.

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	32	DI	USB connection detect	Typical 5.0 V A test point must be reserved.
USB_DP	34	AIO	USB 2.0 differential data (+)	Comply with USB 2.0 specifications. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	33	AIO	USB 2.0 differential data (-)	
USB_SS_TX_M	37	AO	USB 3.0 super-speed transmit (-)	Comply with USB 3.0

USB_SS_TX_P	38	AO	USB 3.0 super-speed transmit (+)	specifications. Require differential impedance of 90 Ω.
USB_SS_RX_P	40	AI	USB 3.0 super-speed receive (+)	
USB_SS_RX_M	41	AI	USB 3.0 super-speed receive (-)	
USB_ID*	36	DI	USB ID detect	If unused, keep it open.
OTG_PWR_EN*	143	DO	OTG power control	

For more details about the USB 2.0 and USB 3.0 specifications, visit http://www.usb.org/home.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in your designs. The following figure shows a reference circuit of USB 2.0 and USB 3.0 interfaces.

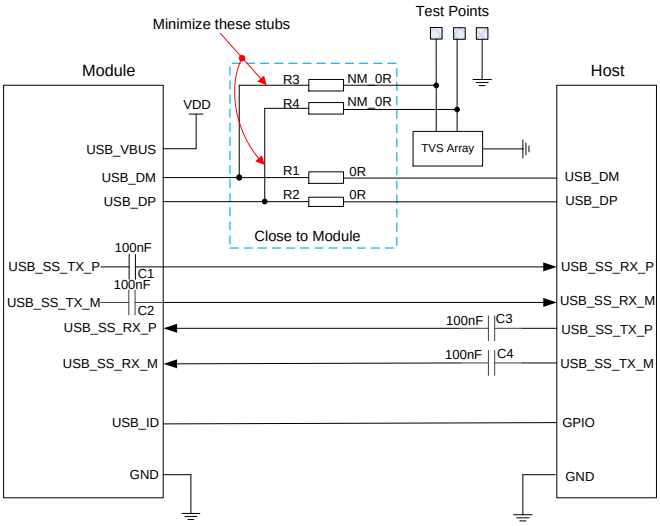


Figure 19: Reference Circuit of USB Application

To ensure the signal integrity of USB data traces, C1, and C2 have already been integrated in the module; C3 and C4 must be placed close to the host; and R1 to R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles of USB interface should be followed during USB interface design to meet USB 2.0 and USB 3.0 specifications.

- Route the USB 2.0 and USB 3.0 signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- For USB 2.0 signal traces, the trace should be shorter than 120 mm, and the differential data pair matching should be less than 2 mm. For USB 3.0 signal traces, the maximum length of each differential data pair (Tx/Rx) is recommended to be less than 100 mm, and each differential data pair matching should be less than 0.7 mm. While the matching between Tx and Rx should be less

than 15.24 mm.

- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is vital to route the USB differential traces in inner-layers of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- If a USB connector is used, keep the ESD protection components as close to the USB connector as possible.
- Pay attention to the selection of the ESD protection component since the component's junction capacitance may cause influences on USB data traces. Typically, the stray capacitance should be less than 2.0 pF for USB 2.0, and less than 0.4 pF for USB 3.0.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces respectively.

Table 14: USB Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)	Length Difference (P-M) (mm)
34	USB_DP	16.02	0.32
33	USB_DM	16.34	
37	USB_SS_TX_M	20.57	0.36
38	USB_SS_TX_P	20.21	
40	USB_SS_RX_P	19.62	0.16
41	USB_SS_RX_M	19.46	

4.3. UART Interfaces

The module provides three UART interfaces: one main UART interface, one debug UART interface, and one Bluetooth UART interface* (multiplexed from SPI). Features of these interfaces are shown as below:

- Main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps (default), 230400 bps, 460800 bps and 921600 bps baud rates. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.
- Bluetooth UART interface supports 115200 bps baud rate. It is used for Bluetooth communication and can be multiplexed from SPI.

4.3.1. Main UART Interface

Table 15: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	56	DO	DCE clear to send signal to DTE	CTS: Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	57	DI	DCE request to send signal from DTE	RTS: Connect to DTE's RTS. If unused, keep it open.
MAIN_RXD	58	DI	Main UART receive	
MAIN_DCD	59	DO	Main UART data carrier detect	
MAIN_TXD	60	DO	Main UART transmit	
MAIN_RI	61	DO	Main UART ring indication	
MAIN_DTR	62	DI	Main UART data terminal ready	Pulled up by default. Pulling low will awaken the module. If unused, keep it open. Sleep mode control.

4.3.2. Debug UART Interface

Table 16: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	136	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	137	DO	Debug UART transmit	

4.3.3. Bluetooth UART Interface*

The module provides one Bluetooth UART interface multiplexed from SPI interface. The following table shows the Bluetooth UART interface pin definition.

Table 17: Pin Definition of Bluetooth UART Interface

Pin Name	Pin No.	Multiplexed Function	I/O	Description	Comment
BT_EN	3	-	DO	Bluetooth function enable control	If unused, keep it open.
SPI_MOSI	163	BT_TXD	DO	Bluetooth UART transmit	
SPI_CLK	164	BT_CTS	DO	DCE clear to send signal to DTE	CTS: Connect to DTE's CTS.
SPI_MISO	165	BT_RXD	DI	Bluetooth UART receive	
SPI_CS	166	BT_RTS	DO	DCE request to send signal from DTE	RTS: Connect to DTE's RTS.

4.3.4. UART Application

The module provides 1.8 V UART interfaces. A level-shifting circuit should be used if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

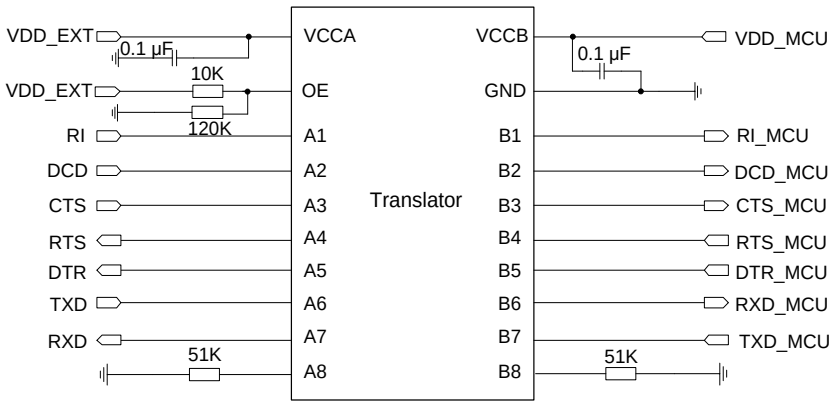


Figure 20: Reference Circuit (IC Solution)

Please visit http://www.ti.com for more information.

Another example with a transistor circuit is shown below. For the design of circuits shown in dotted lines, refer to that shown in solid lines, but pay attention to the direction of the connection.

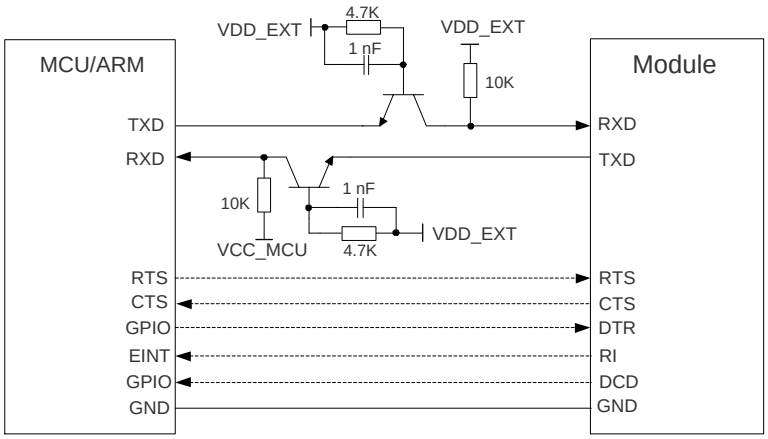


Figure 21: Reference Circuit （Transistor Solution）

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates over 460 kbps.
2. Note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

4.4. SPI

The module provides one SPI which only supports master mode with a maximum clock frequency up to 50 MHz.

Table 18: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_MOSI	163	DO	SPI master output slave input	Master only.
SPI_CLK	164	DO	SPI clock	
SPI_MISO	165	DI	SPI master input slave output	
SPI_CS	166	DO	SPI chip select	

The following figure shows a reference design of PCM interface and SPI with an external SLIC IC. The dotted line in the figure below means an optional connection since some SLIC ICs need RST while some do not.

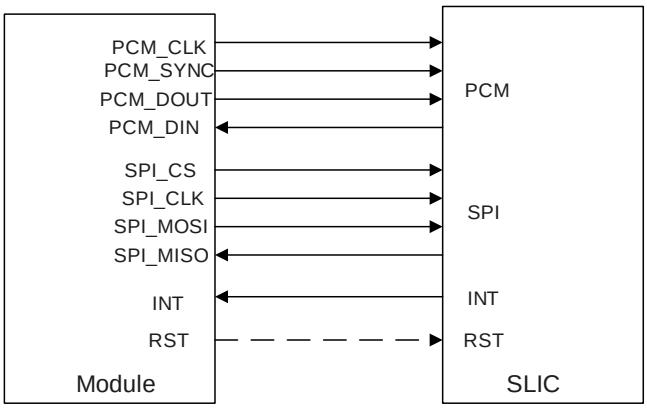


Figure 22: Reference Circuit of PCM and SPI Application with SLIC

4.5. PCM and I2C Interfaces

The module supports audio communication via PCM (Pulse Code Modulation) digital interface and I2C interfaces. The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave.
- Auxiliary mode (long frame synchronization): the module works as master only.

In primary mode, the data is sampled on the falling edge of PCM_CLK and transmitted on the rising edge. The falling edge of PCM_SYNC represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The rising edge of PCM_SYNC represents the MSB. In this mode, the PCM interface operates with 256 kHz PCM_CLK and 8 kHz, 50 % duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

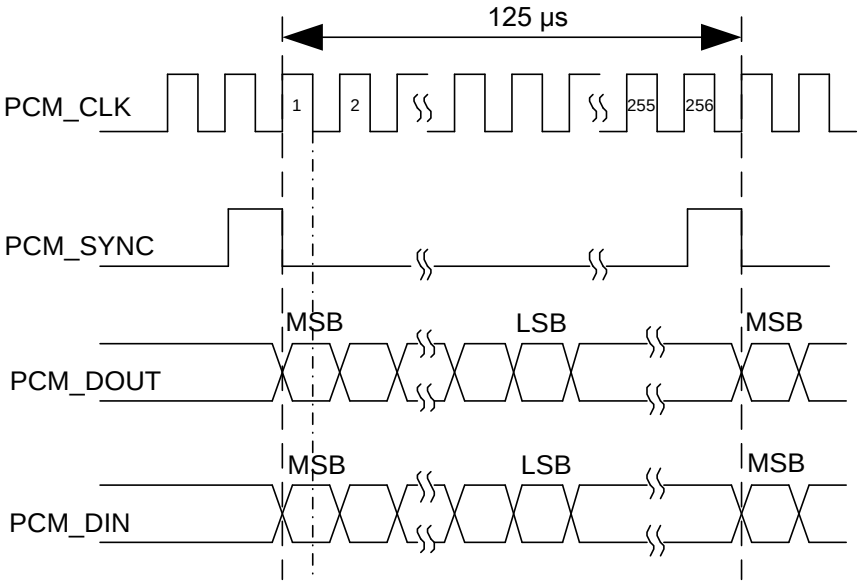


Figure 23: Primary Mode Timing

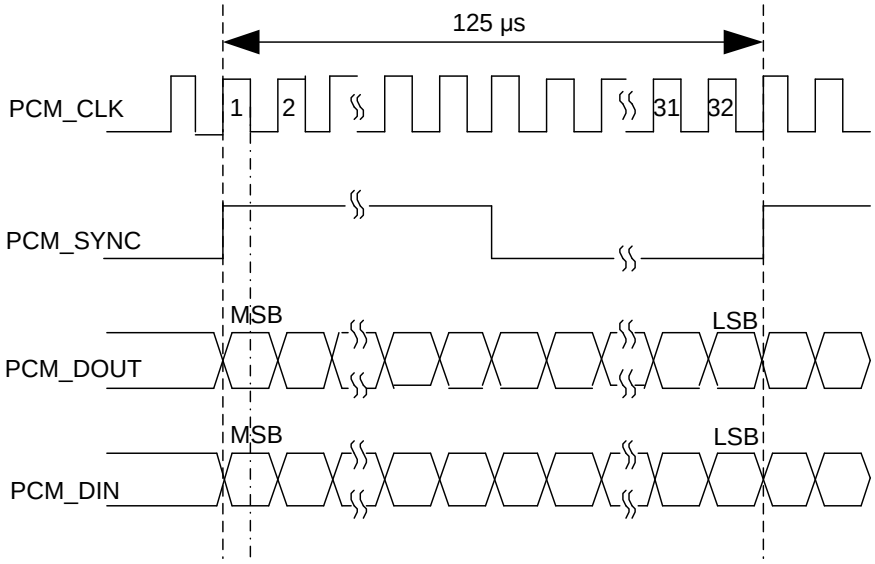


Figure 24: Auxiliary Mode Timing

The following table shows the pin definition of the PCM interface and I2C interface, both of which can be applied to audio codec design.

Table 19: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	66	DI	PCM data input	If unused, keep them open.
PCM_DOUT	68	DO	PCM data output	
PCM_SYNC	65	DIO	PCM data frame sync	Output signal in master mode. Input signal in slave mode. If unused, keep them open.
PCM_CLK	67	DIO	PCM clock	
I2C_SDA	42	OD	I2C serial data (for an external codec)	An external pull-up resistor is requisite. If unused, keep them open.
I2C_SCL	43	OD	I2C serial clock (for an external codec)	
I2S_MCLK	152	DO	Clock output for codec	Provide a digital clock output for an external audio codec. If unused, keep it open. Master only.

Clock and mode can be configured by **AT+QDAI**, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [4]*** for details about the AT command.

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

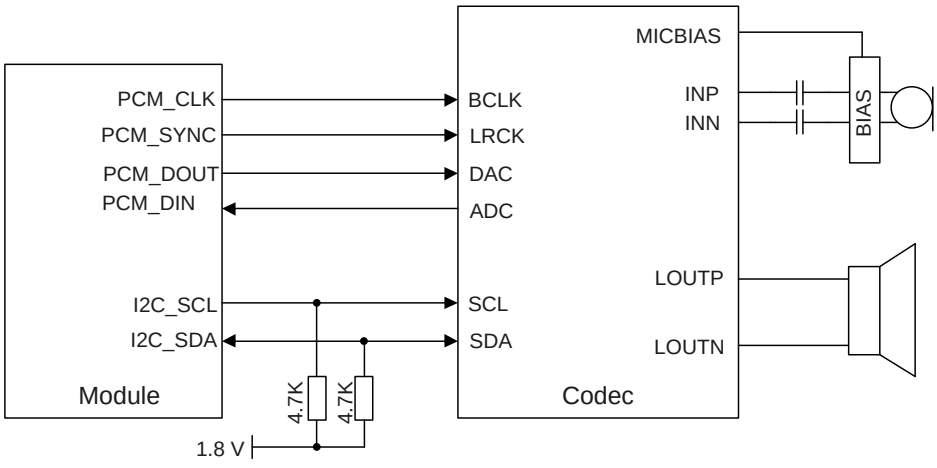


Figure 25: Reference Circuit of PCM and I2C Application with Audio Codec

NOTE

The module works as a master device pertaining to I2C interface.

4.6. ADC Interfaces

The module provides two ADC (Analog-to-Digital Converter) interfaces. Execute **AT+QADC=0** to read the voltage value on ADC0. Execute **AT+QADC=1** to read the voltage value on ADC1. See ***document [4]*** for details about these AT commands.

For higher accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 20: Pin Definition of the ADC Interface

Pin Name	I/O	Pin No.	Description	Comment
ADC0	AI	173	General-purpose ADC interface	0–1.875 V. If unused, keep them open.
ADC1	AI	175		

Table 21: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	1.875	V
ADC1 Voltage Range	0	-	1.875	V
ADC Resolution	-	114.441	-	μV

NOTE

1. The input voltage of ADC should not exceed 1.875 V.
2. It is prohibited to supply any voltage to ADC pins without VBAT.
3. It is recommended to use a resistor divider circuit for ADC application.

4.7. Status Indication

4.7.1. Network Status Indication

The network indication pins NET_MODE and NET_STATUS can be used to drive network status indication LEDs. Their definitions and logic level change upon the switch of network mode/status, which is described in the following tables.

Table 22: Pin Definition of NET_MODE and NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	147	DO	Indicate the module's network registration mode	If unused, keep them open.
NET_STATUS	170	DO	Indicate the module's network activity status	

Table 23: Working Status of NET_MODE and NET_STATUS

Pin Name	Status	Description
NET_MODE	Always High	Registered on network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

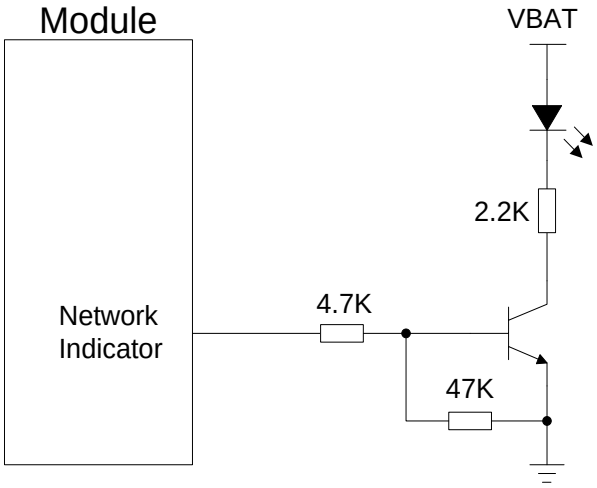


Figure 26: Reference Circuit of the Network Indicator

4.7.2. Module Status Indication

The STATUS pin is set as the module's status indicator. It outputs high-level voltage when the module is turned on.

Table 24: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	171	DO	Indicate the module's operation status	If unused, keep it open.

A reference circuit is shown as below.

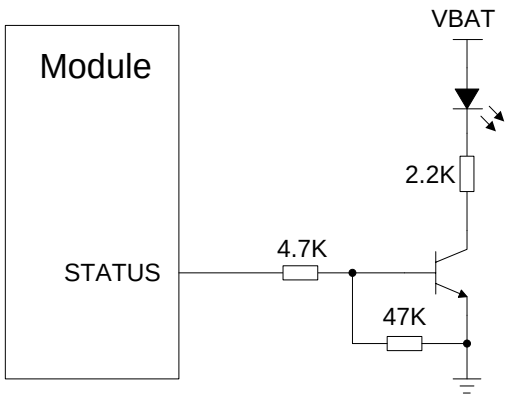


Figure 27: Reference Circuits of STATUS

4.8. RI

Execute **AT+QCFG="risignaltype","physical"** to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI. The behavior of MAIN_RI can be altered by executing **AT+QCFG="urc/ri/ring"**. See ***document [4]*** for details about these AT commands.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 25: Default Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at a high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

NOTE

The URC can be output from UART port, USB AT port (by default) and USB modem port by executing **AT+QURCCFG**. See ***document [4]*** for details about the AT command.

4.9. PCIe Interface

The module provides one integrated PCIe (Peripheral Component Interconnect Express) interface which can transmit data. The module supports PCIe Root Complex (RC) mode only.

- *PCI Express Base Specification Revision 2.0* compliant
- Data rate up to 5 Gbps/lane
- Can be connected to an external Ethernet IC (MAC and PHY) or WLAN IC

Table 26: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	179	AO	PCIe reference clock (+)	Require differential impedance of 95 Ω. If unused, keep them open.
PCIE_REFCLK_M	180	AO	PCIe reference clock (-)	
PCIE_TX_M	182	AO	PCIe transmit (-)	

PCIE_TX_P	183	AO	PCIe transmit (+)	
PCIE_RX_M	185	AI	PCIe receive (-)	
PCIE_RX_P	186	AI	PCIe receive (+)	
PCIE_CLKREQ_N	188	DI	PCIe clock request	Input signal in master mode. If unused, keep it open.
PCIE_RC_RST_N	189	DO	PCIe RC reset	Output signal in master mode. If unused, keep it open.
PCIE_WAKE_N	190	DI	PCIe awake	Input signal, in master mode only. If unused, keep it open.

To enhance the reliability and availability in applications, follow the criteria below in the PCIe interface circuit design:

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and clock signals.
- Add a capacitor in series on Rx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length matching of each differential data pair (Tx/Rx/REFCLK) less than 0.7 mm for PCIe routing traces.
- Keep the differential impedance of PCIe data trace as 85 Ω ±10%.
- Do not route PCIe data traces under components or cross them with other traces.

The module only supports Root Complex (RC) mode. In this mode, the module is configured to act as a PCIe RC device. The following figure shows a reference circuit of PCIe RC mode.

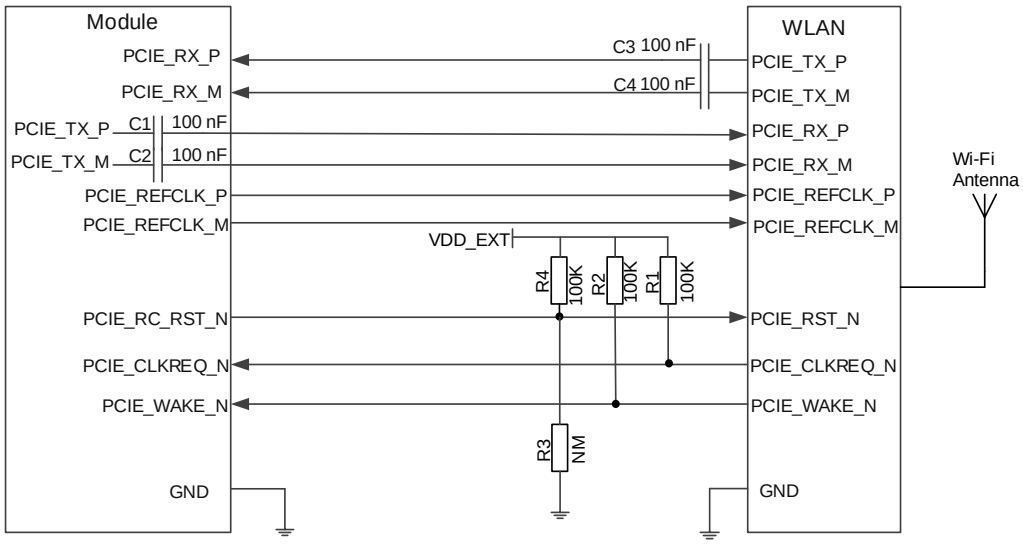


Figure 28: PCIe Interface Reference Circuit (RC Mode)

Table 27: PCIe Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)	Length Difference (P-M) (mm)
179	PCIE_REFCLK_P	22.24	0.10
180	PCIE_REFCLK_M	22.14	
182	PCIE_TX_M	17.99	0.08
183	PCIE_TX_P	17.91	
185	PCIE_RX_M	13.91	0.07
186	PCIE_RX_P	13.98	

4.10. SDIO Interface

The module provides one SDIO interface which supports SD 3.0 protocol. The following table shows the pin definition.

Table 28: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
VDD_P2	135	PI	Power input for SDIO interface	If a SD card is used, connect VDD_P2 to SDIO_VDD. If unused, connect VDD_P2 to VDD_EXT.
SDIO_VDD	46	PO	SD card application: SDIO pull up power source	Cannot work as SD card power supply. SD card must be powered by an external power supply.
SDIO_DATA3	48	DIO	SDIO data bit 3	If unused, keep them open.
SDIO_DATA2	47	DIO	SDIO data bit 2	
SDIO_DATA1	50	DIO	SDIO data bit 1	
SDIO_DATA0	49	DIO	SDIO data bit 0	
SDIO_CMD	51	DIO	SDIO command	

SDIO_DET	52	DI	SD card detect
SDIO_CLK	53	DO	SDIO clock

The following figure shows an SDIO interface reference design.

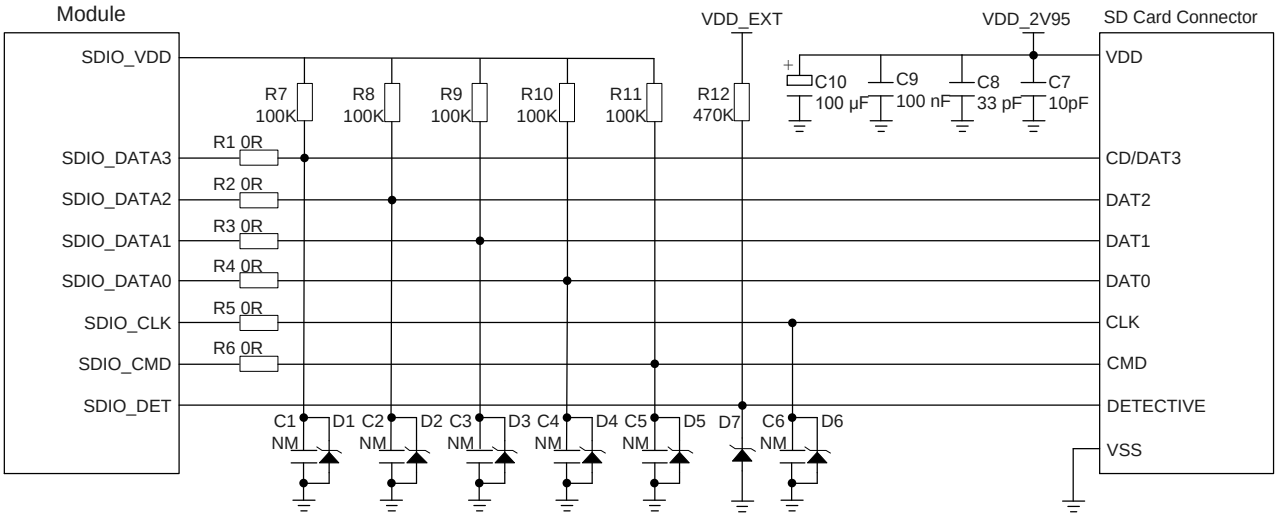


Figure 29: Reference Circuit of SD Card Application

Follow the principles below in the SD card circuit design:

- The voltage of SD power supply ranges from 2.7 V to 3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of SDIO_VDD is 50 mA which can only work as SDIO pull-up resistors, the SD card needs an external power supply.
- To avoid the jitter, resistors R7 to R11 are needed to pull up the SDIO signals to SDIO_VDD. The values of these resistors range from 10 kΩ to 100 kΩ and the preferred value is 100 kΩ.
- To improve signal quality, it is recommended to add resistors R1 to R6 of 0 Ω in series between the module and the SD card connector. The bypass capacitors C1 to C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- For better ESD protection, it is recommended to add a TVS array on each SD signal trace.
- It is important to route the SDIO signal traces with ground. The impedance of SDIO data trace is 50 Ω (± 10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, and analog signals, as well as noise signals such as clock signals and DC-DC signals.
- It is recommended to keep the trace length difference between SDIO_CLK and SDIO_DATA/SDIO_CMD within 1 mm and the total routing length less than 50 mm. The trace inside the module is 25 mm long in total, so the exterior trace should be less than 25 mm in total.
- Make sure the adjacent trace spacing is twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.

4.11. Antenna Tuner Control Interfaces*

The module supports external antenna tuner control through the RFFE interface. The following is the pin definition of the RFFE interfaces.

Table 29: Pin Definition of RFFE Interfaces

Pin Name	Pin No.	I/O	Description	Comment
RFFE_CLK	71	DO	RFFE serial interface for external antenna tuner control.	If unused, keep them open.
RFFE_DATA	73	DIO		

4.12. USB_BOOT Interface

The module provides one USB_BOOT pin. Pull up USB_BOOT to VDD_EXT before turning on the module, then the module will enter emergency download mode when turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 30: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	140	DI	Force the module into emergency download mode	Active high. A test point is recommended to be reserved.

The following figure shows a reference circuit of USB_BOOT.

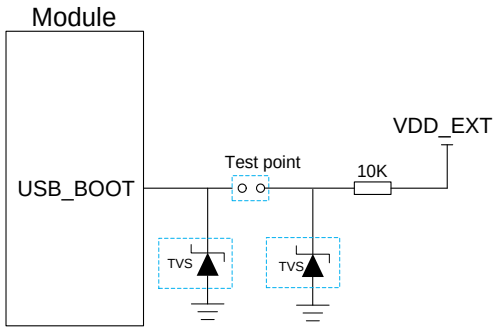


Figure 30: Reference Circuit of USB_BOOT

5 RF Specifications

The module provides one main antenna interface, one Rx-diversity antenna interface, two MIMO antenna interfaces, and one GNSS antenna interface. The impedance of antenna port is 50 Ω.

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The pin definition of main antenna interface, Rx-diversity antenna interface and MIMO antenna interfaces are shown as below.

Table 31: Pin Definition of the Main/Rx-diversity/MIMO Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	107	AIO	Main antenna interface	50 Ω impedance
ANT1	127	AI	Rx-diversity antenna interface	
ANT2	101	AI	4 × 4 MIMO antenna interface	
ANT3	113	AI		

Table 32: Frequency Bands

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz

WCDMA B3	1710–1785	1805–1880	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
LTE B1	1920–1980	2110–2170	MHz
LTE B2	1850–1910	1930–1990	MHz
LTE B3	1710–1785	1805–1880	MHz
LTE B4	1710–1755	2110–2155	MHz
LTE B5	824–849	869–894	MHz
LTE B7	2500–2570	2620–2690	MHz
LTE B8	880–915	925–960	MHz
LTE B12	699–716	729–746	MHz
LTE B13	777–787	746–756	MHz
LTE B14	788–798	758–768	MHz
LTE B20	832–862	791–821	MHz
LTE B25	1850–1915	1930–1995	MHz
LTE B26	814–849	859–894	MHz
LTE B28	703–748	758–803	MHz
LTE B29	-	717–728	MHz
LTE B30	2305–2315	2350–2360	MHz
LTE B32	-	1452–1496	MHz
LTE B38	2570–2620	2570–2620	MHz
LTE B40	2300–2400	2300–2400	MHz
LTE B41	2496–2690	2496–2690	MHz
LTE B42	3400–3600	3400–3600	MHz

LTE B43	3600–3800	3600–3800	MHz
LTE B48	3550–3700	3550–3700	MHz
LTE B66	1710–1780	2110–2200	MHz
LTE B71	663–698	617–652	MHz

5.1.2. Tx Power

Table 33: Tx Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
WCDMA bands	23 dBm ±2 dB	< -50 dBm
LTE bands	23 dBm ±2 dB	< -40 dBm

5.1.3. Rx Sensitivity

Table 34: EG060K-EA & EG120K-EA Dual-Antenna Conducted RF Rx Sensitivity

Frequency Band	Primary	Diversity	SIMO [8]	3GPP (SIMO)	Unit
WCDMA B1	-107.5	-107.5	-109.8	-106.7	dBm
WCDMA B3	-109.5	-109.5	-111	-103.7	dBm
WCDMA B5	-109.5	-110	-112.5	-104.7	dBm
WCDMA B8	-109.5	-110	-112.5	-103.7	dBm
LTE-FDD B1 (10 MHz)	-96	-96	-98.5	-96.3	dBm
LTE-FDD B3 (10 MHz)	-97.2	-97.3	-100.2	-93.3	dBm
LTE-FDD B5 (10 MHz)	-97	-99	-101	-94.3	dBm
LTE-FDD B7 (10 MHz)	-96.5	-96	-99.2	-94.3	dBm
LTE-FDD B8 (10 MHz)	-97.5	-99	-101	-93.3	dBm

[8] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and multiple (Primary + Diversity or Primary + Diversity + MIMO1 + MIMO2) antennas at the receiver side, which can improve Rx performance. Rx sensitivity values are measured in four antennas condition (Primary + Diversity or Primary + Diversity + MIMO1 + MIMO2).

LTE-FDD B20 (10 MHz)	-97.2	-99.2	-101.2	-93.3	dBm
LTE-FDD B28 (10 MHz)	-98.1	-99.5	-101.5	-94.8	dBm
LTE-FDD B32 (10 MHz) [9]	-96.4	-96.5	-99	-96.3	dBm
LTE-TDD B38 (10 MHz)	-96.3	-96.4	-98.8	-96.3	dBm
LTE-TDD B40 (10 MHz)	-96	-96	-98.2	-96.3	dBm
LTE-TDD B41 (10 MHz)	-95.8	-96	-98.5	-94.3	dBm
LTE-TDD B42 (10 MHz)	-97.2	-96.9	-99.3	-95	dBm
LTE-TDD B43 (10 MHz)	-96.5	-98.7	-98.5	-95	dBm

Table 35: EG060K-NA & EG120K-NA Dual-Antenna Conducted RF Rx Sensitivity

Frequency Band	Primary	Diversity	SIMO [8]	3GPP (SIMO)	Unit
LTE-FDD B2 (10 MHz)	-97	-95.3	-99.2	-94.3	dBm
LTE-FDD B4 (10 MHz)	-96	-96	-98.4	-96.3	dBm
LTE-FDD B5 (10 MHz)	-97.1	-99	-100.5	-94.3	dBm
LTE-FDD B7 (10 MHz)	-95.1	-95	-98	-94.3	dBm
LTE-FDD B12 (10 MHz)	-98	-99.5	-101.7	-93.3	dBm
LTE-FDD B13 (10 MHz)	-98	-99.5	-101	-93.3	dBm
LTE-FDD B14 (10 MHz)	-98	-99.7	-101.4	-93.3	dBm
LTE-FDD B25 (10 MHz)	-97	-95.3	-99	-92.8	dBm
LTE-FDD B26 (10 MHz)	-97	-99.1	-101	-93.8	dBm
LTE-FDD B29 (10 MHz) [10]	-98	-98.3	-101.1	-93.3	dBm
LTE-FDD B30 (10 MHz)	-95	-95.3	-97.5	-95.3	dBm
LTE-TDD B41 (10 MHz)	-95.2	-95	-98	-94.3	dBm
LTE-TDD B48 (10 MHz)	-96.5	-98.2	-100.2	-95	dBm

[9] The test results are based on CA_20A-32A.
[10] The test results are based on CA_2A-29A.

LTE-FDD B66 (10 MHz)	-96	-96	-98.3	-95.8	dBm
LTE-FDD B71 (10 MHz)	-98.2	-100	-102	-94.3	dBm

Table 36: EG060K-LA & EG120K-LA Dual-Antenna Conducted RF Rx Sensitivity

Frequency Band	Primary	Diversity	SIMO [8]	3GPP (SIMO)	Unit
WCDMA B2	-110	-110.5	-112.7	-104.7	dBm
WCDMA B4	-108.5	-108.4	-109.3	-106.7	dBm
WCDMA B5	-110	-111.4	-112.1	-104.7	dBm
WCDMA B8	-110	-110.3	-111	-103.7	dBm
LTE-FDD B2 (10 MHz)	-97	-95.3	-99.2	-94.3	dBm
LTE-FDD B4 (10 MHz)	-96	-96	-98.6	-96.3	dBm
LTE-FDD B5 (10 MHz)	-97	-99	-100.5	-94.3	dBm
LTE-FDD B7 (10 MHz)	-96.5	-96	-99.2	-94.3	dBm
LTE-FDD B8 (10 MHz)	-97.5	-99	-101	-93.3	dBm
LTE-FDD B25 (10 MHz)	-97	-95.3	-99	-92.8	dBm
LTE-FDD B28 (10 MHz)	-98.1	-99.5	-100.7	-94.8	dBm
LTE-FDD B66 (10 MHz)	-96	-96	-98.3	-96.5	dBm
LTE-TDD B42 (10 MHz)	-96	-96.7	-96.8	-95	dBm
LTE-TDD B43 (10 MHz)	-96.1	-99.3	-100.8	-95	dBm

Table 37: EG120K-EA Four-Antenna Conducted RF Rx Sensitivity

Frequency Band	SIMO (dBm) [8]	3GPP (SIMO)	Unit
LTE-FDD B1 (10 MHz)	-101.7	-99	dBm
LTE-FDD B3 (10 MHz)	-102.5	-96	dBm
LTE-FDD B7 (10 MHz)	-101	-97	dBm

LTE-TDD B38 (10 MHz)	-102	-	dBm
LTE-TDD B40 (10 MHz)	-101.5	-99	dBm
LTE-TDD B41 (10 MHz)	-101.5	-97	dBm
LTE-TDD B42 (10 MHz)	-104.3	-	dBm

Table 38: EG060K-NA & EG120K-NA Four-Antenna Conducted RF Rx Sensitivity

Frequency Band	SIMO (dBm) [8]	3GPP (SIMO)	Unit
LTE-FDD B2 (10 MHz)	-103	-97	dBm
LTE-FDD B4 (10 MHz)	-102.1	-99	dBm
LTE-FDD B7 (10 MHz)	-102	-97	dBm
LTE-FDD B25 (10 MHz)	-103	-95.5	dBm
LTE-FDD B30 (10 MHz)	-101	-	dBm
LTE-TDD B41 (10 MHz)	-101.7	-97	dBm
LTE-TDD B48 (10 MHz)	-104	-	dBm
LTE-FDD B66 (10 MHz)	-102.1	-98.5	dBm

Table 39: EG060K-LA & EG120K-LA Four-Antenna Conducted RF Rx Sensitivity

Frequency Band	SIMO (dBm) [8]	3GPP (SIMO)	Unit
LTE-FDD B2 (10 MHz)	-103	-97	dBm
LTE-FDD B4 (10 MHz)	-102.1	-99	dBm
LTE-FDD B7 (10 MHz)	-102	-97	dBm
LTE-FDD B25 (10 MHz)	-103.3	-95.5	dBm
LTE-FDD B66 (10 MHz)	-102.3	-98.5	dBm
LTE-TDD B42 (10 MHz)	-101.1	-	dBm

5.1.4. Reference Design

A reference design of ANT0, ANT1, ANT2 and ANT3 interfaces is shown as below. It requires a π-type matching circuit for better RF performance. The π-type matching components (R1/C1/C2, R2/C3/C4, R3/C5/C6, R4/C7/C8) should be placed as close to the antennas as possible and are mounted according to the actual debugging. C1 to C8 are not mounted and a 0 Ω resistor is mounted on R1 to R4 respectively by default.

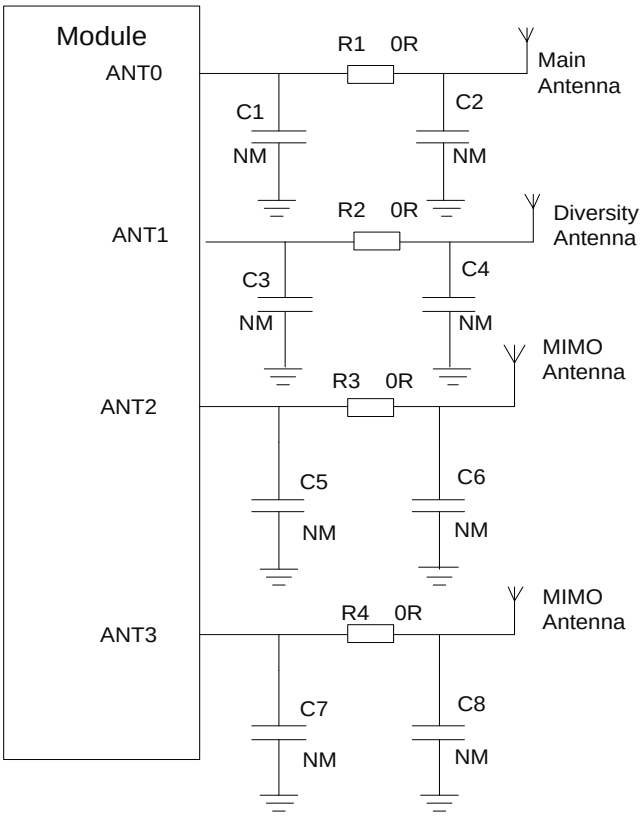


Figure 31: Reference Circuit of RF Antenna Interfaces

NOTE

Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.

5.2. GNSS

5.2.1. Antenna Interface & Frequency Bands

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, and Galileo. The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the module GNSS engine is off. It must be switched on via AT command. For more details, see ***document [4]***.

Table 40: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	119	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 41: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz

5.2.2. GNSS Performance

Table 42: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-147	dBm
	Reacquisition	Autonomous	-159	dBm
	Tracking	Autonomous	-159	dBm
TTFF	Cold start	Autonomous	30	s

	@ open sky	XTRA enabled	10	s
	Warm start @ open sky	Autonomous	27	s
		XTRA enabled	3	s
	Hot start @ open sky	Autonomous	1.1	s
		XTRA enabled	1.1	s
Accuracy	CEP-50	Autonomous @ open sky	2	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Passive Antenna Reference Design

GNSS Antenna interface supports passive ceramic antenna or other types of passive antennas. The reference design of GNSS passive antenna is shown as below.

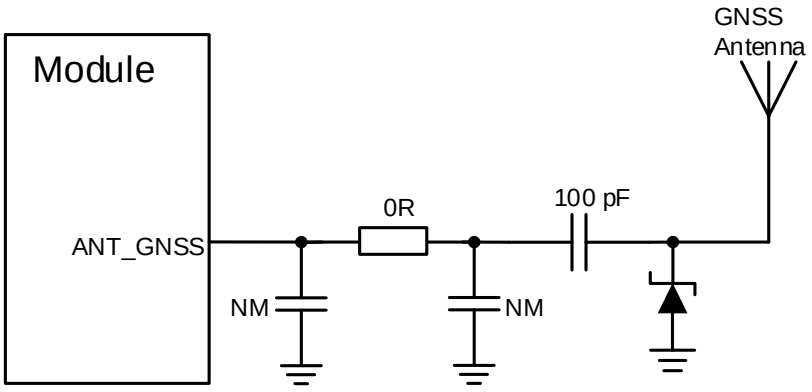


Figure 32: Reference Circuit of GNSS Passive Antenna Interface

NOTE

1. An external LDO can be used to supply power according to the active antenna requirements.
2. The VDD circuit is unnecessary if the module is equipped with a passive antenna.
3. It is not recommended to add an external LNA when using a passive GNSS antenna.

5.2.4. Active Antenna Reference Design

GNSS Antenna interface also supports active antenna. In any case, it is recommended to use a passive antenna. If active antenna is indeed needed in your application, it is recommended to reserve a π-type attenuation circuit provision and use high-performance LDO as the power supply. The reference design of GNSS passive antenna is shown as below.

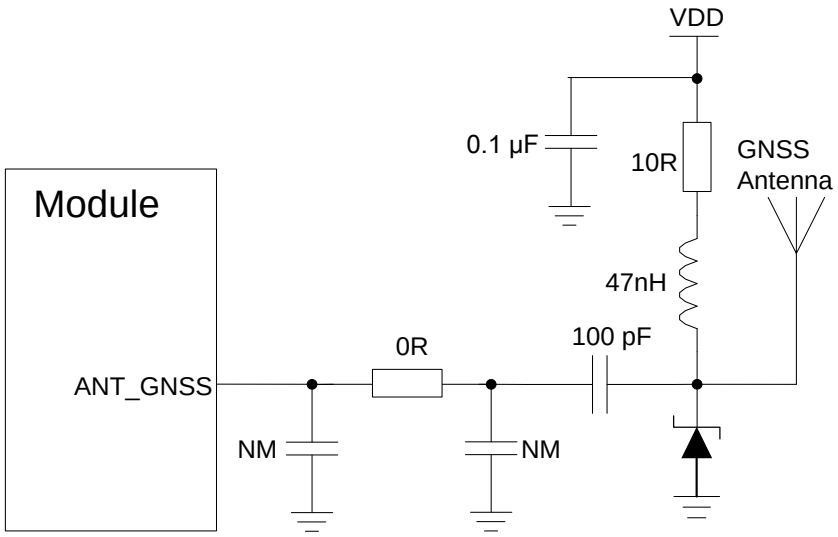


Figure 33: Reference Circuit of GNSS Active Antenna Interface

5.3. RF Routing Guidelines

For the PCB, control the characteristic impedance of all RF traces to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

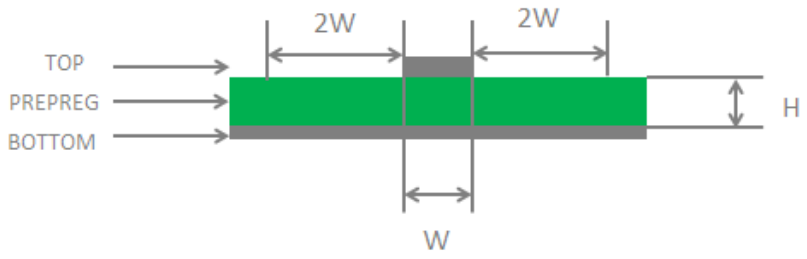


Figure 34: Microstrip Line Design on a 2-layer PCB

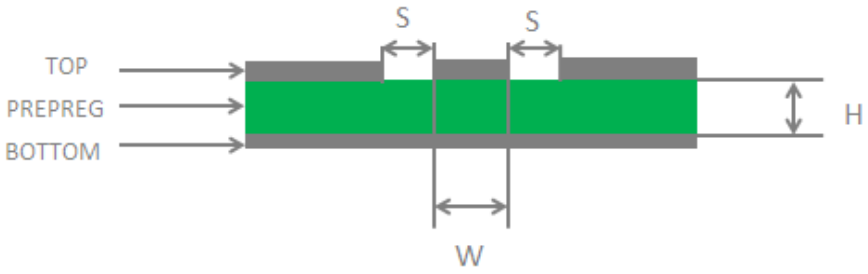


Figure 35: Coplanar Waveguide Line Design on a 2-layer PCB

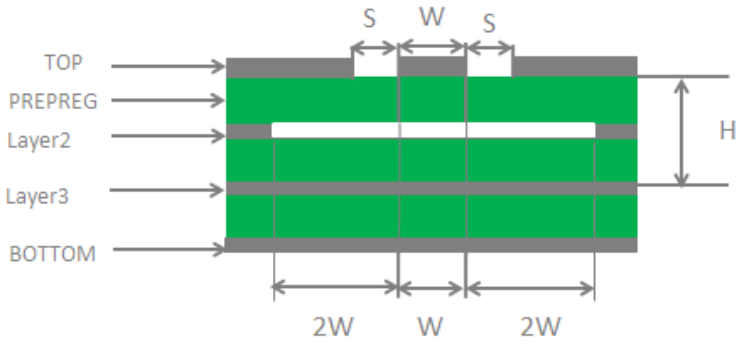


Figure 36: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

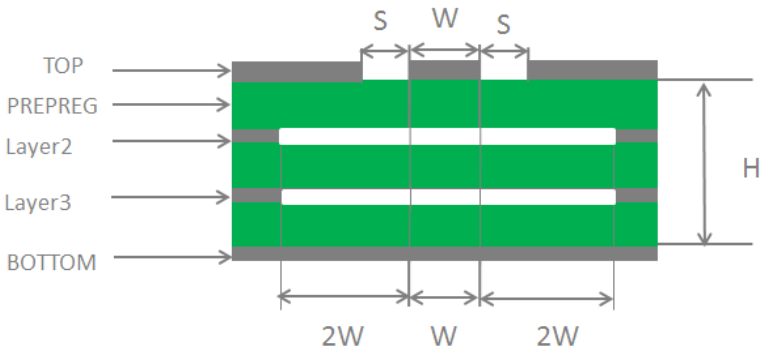


Figure 37: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- Reserve clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice of the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [5]***.

5.4. Antenna Design Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 43: Antenna Design Requirements

Antenna Type	Requirements
GNSS	● Frequency range: 1559–1609 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.)
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
WCDMA/LTE	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: – **< 1 dB:** LB (<1 GHz) – **< 1.5 dB:** MB (1–2.3 GHz) – **< 2 dB:** HB (> 2.3 GHz)

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

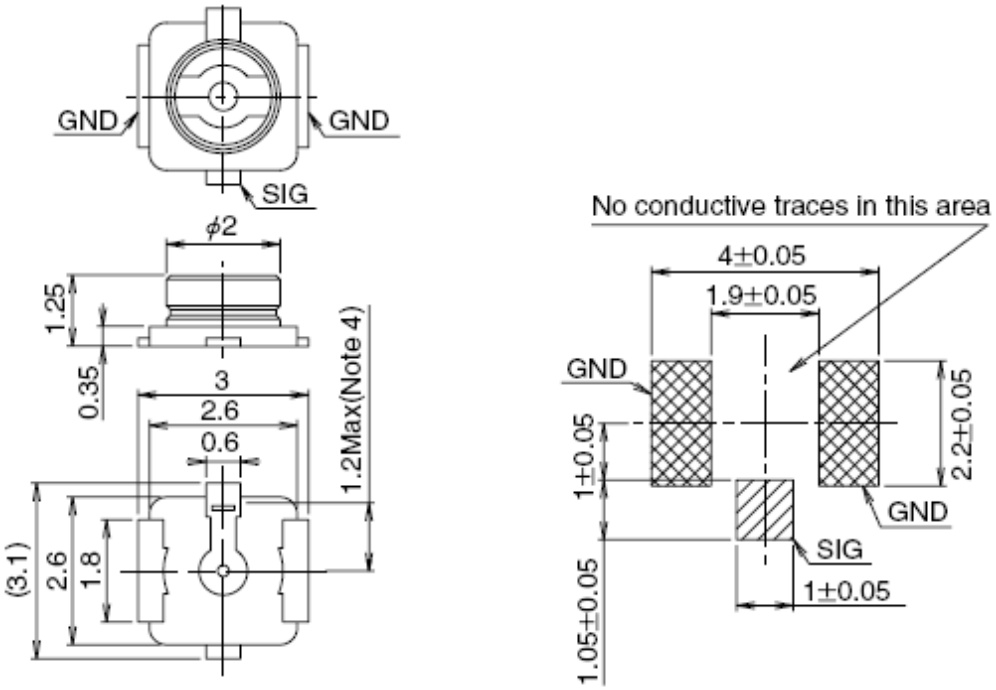


Figure 38: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

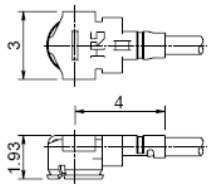
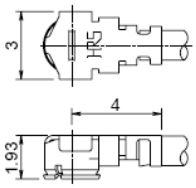
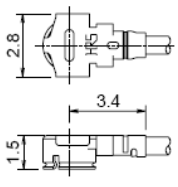
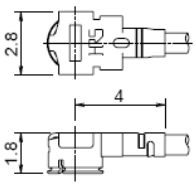
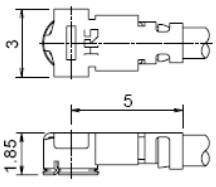
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Specifications of Mated Plugs

The following figure describes the space factor of mated plugs.

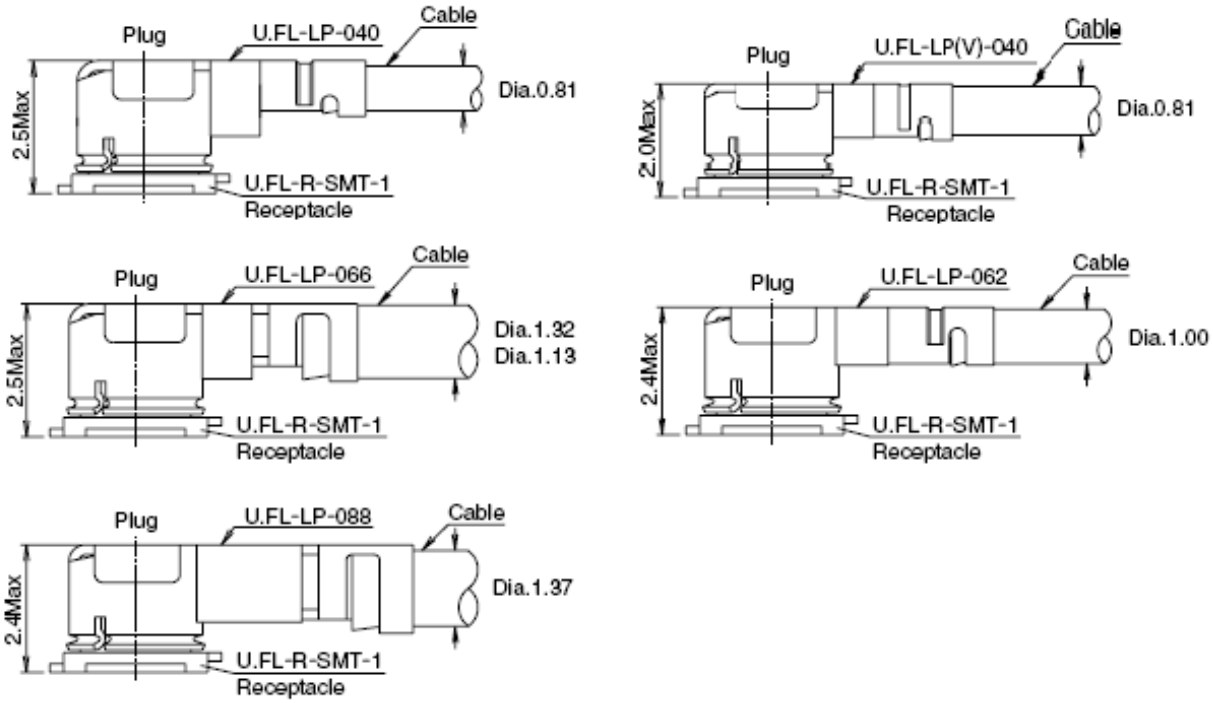


Figure 40: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 44: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.0	A
Peak Current of VBAT_RF	-	1.2	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC	-0.5	2.3	V

6.2. Power Supply Ratings

Table 45: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.4	V
USB_VBUS	USB connection detection	-	3.3	5.0	5.25	V

6.3. Power Consumption

Table 46: EG060K-EA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.22	mA
	WCDMA PF = 64 (USB disconnected)	2.55	mA
	WCDMA PF = 128 (USB disconnected)	2.01	mA
	WCDMA PF = 512 (USB disconnected)	1.51	mA
	LTE-FDD PF = 32 (USB disconnected)	4.49	mA
	LTE-FDD PF = 64 (USB disconnected)	3.68	mA
	LTE-FDD PF = 128 (USB disconnected)	2.71	mA
	LTE-TDD PF = 32 (USB disconnected)	4.82	mA
	LTE-TDD PF = 64 (USB disconnected)	3.95	mA
	LTE-TDD PF = 128 (USB disconnected)	2.90	mA
Idle state	WCDMA PF = 64 (USB disconnected)	11.02	mA

	WCDMA PF = 64 (USB 2.0 connected)	17.43	mA
	LTE-FDD PF = 64 (USB disconnected)	11.51	mA
	LTE-FDD PF = 64 (USB 2.0 connected)	17.71	mA
	LTE-TDD PF = 64 (USB disconnected)	11.94	mA
	LTE-TDD PF = 64 (USB 2.0 connected)	18.20	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH10700 @ 22.22 dBm	559	mA
	WCDMA B1 HSUPA CH10700 @ 21.34 dBm	516	mA
	WCDMA B3 HSDPA CH1338 @ 22.31 dBm	609	mA
	WCDMA B3 HSUPA CH1338 @ 21.53 dBm	565	mA
	WCDMA B5 HSDPA CH4407 @ 22.29 dBm	550	mA
	WCDMA B5 HSUPA CH4407 @ 21.49 dBm	522	mA
	WCDMA B8 HSDPA CH3012 @ 22.27 dBm	635	mA
	WCDMA B8 HSUPA CH3012 @ 21.62 dBm	563	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH300 @ 22.81 dBm	749	mA
	LTE-FDD B3 CH1575 @ 23.42 dBm	743	mA
	LTE-FDD B5 CH2525 @ 22.94 dBm	583	mA
	LTE-FDD B7 CH3100 @ 23.18 dBm	684	mA
	LTE-FDD B8 CH3625 @ 22.91 dBm	688	mA
	LTE-FDD B20 CH6300 @ 22.95 dBm	713	mA
	LTE-FDD B28 CH27460 @ 22.93 dBm	658	mA
	LTE-TDD B38 CH38000 @ 23.21 dBm	421	mA
	LTE-TDD B40 CH39150 @ 23.14 dBm	440	mA
	LTE-TDD B41 CH40740 @ 23.06 dBm	415	mA
	LTE-TDD B42 CH42590 @ 23.05 dBm	417	mA
	LTE-TDD B43 CH43690 @ 22.9 dBm	312	mA

WCDMA voice call	WCDMA B1 CH10700 @ 23.12 dBm	601	mA
	WCDMA B3 CH1338 @ 23.17 dBm	657	mA
	WCDMA B5 CH4407 @ 23.24 dBm	606	mA
	WCDMA B8 CH3012 @ 23.23 dBm	698	mA

Table 47: EG120K-EA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
	WCDMA PF = 64 (USB disconnected)	2.71	mA
	WCDMA PF = 128 (USB disconnected)	2.11	mA
	WCDMA PF = 512 (USB disconnected)	1.64	mA
	LTE-FDD PF = 32 (USB disconnected)	4.32	mA
	LTE-FDD PF = 64 (USB disconnected)	3.36	mA
	LTE-FDD PF = 128 (USB disconnected)	1.88	mA
	LTE-TDD PF = 32 (USB disconnected)	4.1	mA
	LTE-TDD PF = 64 (USB disconnected)	3.65	mA
	LTE-TDD PF = 128 (USB disconnected)	2.00	mA
Idle state	WCDMA PF = 64 (USB disconnected)	9.83	mA
	WCDMA PF = 64 (USB 2.0 connected)	16.10	mA
	LTE-FDD PF = 64 (USB disconnected)	10.15	mA
	LTE-FDD PF = 64 (USB 2.0 connected)	16.46	mA
	LTE-TDD PF = 64 (USB disconnected)	10.97	mA
	LTE-TDD PF = 64 (USB 2.0 connected)	16.55	mA
WCDMA data	WCDMA B1 HSDPA CH10700 @ 22.08 dBm	544	mA

transfer (GNSS OFF)	WCDMA B1 HSUPA CH10700 @ 20.88 dBm	503	mA
	WCDMA B3 HSDPA CH1338 @ 22.02 dBm	636	mA
	WCDMA B3 HSUPA CH1338 @ 21.21 dBm	590	mA
	WCDMA B5 HSDPA CH4407 @ 22.17 dBm	516	mA
	WCDMA B5 HSUPA CH4407 @ 21.44 dBm	497	mA
	WCDMA B8 HSDPA CH3012 @ 22.21 dBm	614	mA
	WCDMA B8 HSUPA CH3012 @ 20.94 dBm	553	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH300 @ 22.78 dBm	695	mA
	LTE-FDD B3 CH1575 @ 22.73 dBm	760	mA
	LTE-FDD B5 CH2525 @ 22.96 dBm	572	mA
	LTE-FDD B7 CH3100 @ 23.13 dBm	782	mA
	LTE-FDD B8 CH3625 @ 22.81 dBm	669	mA
	LTE-FDD B20 CH6300 @ 22.87 dBm	684	mA
	LTE-FDD B28 CH27460 @ 22.93 dBm	628	mA
	LTE-TDD B38 CH38000 @ 23.09 dBm	396	mA
	LTE-TDD B40 CH39150 @ 22.9 dBm	489	mA
	LTE-TDD B41 CH40740 @ 22.88 dBm	443	mA
	LTE-TDD B42 CH42590 @22.24 dBm	367	mA
	LTE-TDD B43 CH43690 @22.14 dBm	287	mA
WCDMA voice call	WCDMA B1 CH10700 @ 23.01 dBm	598	mA
	WCDMA B3 CH1338 @ 23.04 dBm	688	mA
	WCDMA B5 CH4407 @ 23.18 dBm	571	mA
	WCDMA B8 CH3012 @ 23.15 dBm	693	mA

Table 48: EG060K-NA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
	LTE-FDD PF = 32 (USB disconnected)	3.99	mA
	LTE-FDD PF = 64 (USB disconnected)	2.65	mA
	LTE-FDD PF = 128 (USB disconnected)	1.99	mA
	LTE-FDD PF = 256 (USB disconnected)	1.76	mA
	LTE-TDD PF = 32 (USB disconnected)	4.27	mA
	LTE-TDD PF = 64 (USB disconnected)	2.83	mA
	LTE-TDD PF = 128 (USB disconnected)	2.1	mA
	LTE-TDD PF = 256 (USB disconnected)	1.75	mA
Idle state	LTE-FDD PF = 64 (USB disconnected)	11.52	mA
	LTE-FDD PF = 64 (USB 2.0 connected)	18.71	mA
	LTE-TDD PF = 64 (USB disconnected)	11.87	mA
	LTE-TDD PF = 64 (USB 2.0 connected)	18.83	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 CH1100 @ 22.82 dBm	732	mA
	LTE-FDD B4 CH2050 @ 22.74 dBm	760	mA
	LTE-FDD B5 CH2525 @ 23.0 dBm	597	mA
	LTE-FDD B7 CH3100 @ 22.61 dBm	779	mA
	LTE-FDD B12 CH5095 @ 22.95 dBm	636	mA
	LTE-FDD B13 CH5230@ 22.84 dBm	623	mA
	LTE-FDD B14 CH5330 @ 22.97 dBm	577	mA
	LTE-FDD B25 CH8590 @ 22.83 dBm	711	mA
	LTE-FDD B26 CH8765 @ 22.94 dBm	631	mA

	LTE-FDD B30 CH9820 @ 22.5 dBm	897	mA
	LTE-TDD B41 CH40620 @ 22.75 dBm	453	mA
	LTE-TDD B48 CH55340 @ 22.67 dBm	426	mA
	LTE-FDD B66 CH66536 @ 23.07 dBm	745	mA
	LTE-FDD B71 CH68686 @ 22.94 dBm	751	mA

Table 49: EG120K-NA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
	LTE-FDD PF = 32 (USB disconnected)	3.9	mA
	LTE-FDD PF = 64 (USB disconnected)	3.4	mA
	LTE-FDD PF = 128 (USB disconnected)	1.9	mA
	LTE-FDD PF = 256 (USB disconnected)	1.6	mA
	LTE-TDD PF = 32 (USB disconnected)	4.4	mA
	LTE-TDD PF = 64 (USB disconnected)	3.1	mA
	LTE-TDD PF = 128 (USB disconnected)	2.3	mA
	LTE-TDD PF = 256 (USB disconnected)	2.0	mA
Idle state	LTE-FDD PF = 64 (USB disconnected)	10.2	mA
	LTE-FDD PF = 64 (USB 2.0 connected)	20	mA
	LTE-TDD PF = 64 (USB disconnected)	15	mA
	LTE-TDD PF = 64 (USB 2.0 connected)	22	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 CH1100 @ 23.08 dBm	749	mA
	LTE-FDD B4 CH2050 @ 22.91 dBm	757	mA
	LTE-FDD B5 CH2525 @ 23.16 dBm	598	mA

	LTE-FDD B7 CH3100 @ 22.9 dBm	815	mA
	LTE-FDD B12 CH5060 @ 22.95 dBm	634	mA
	LTE-FDD B13 CH5230 @ 22.93 dBm	608	mA
	LTE-FDD B14 CH5330 @ 23.08 dBm	568	mA
	LTE-FDD B25 CH8590 @ 23.15 dBm	752	mA
	LTE-FDD B26 CH8765 @ 23.12 dBm	644	mA
	LTE-FDD B30 CH9820 @ 22.63 dBm	946	mA
	LTE-TDD B41 CH40620 @ 23.07 dBm	433	mA
	LTE-TDD B48 CH56640 @ 22.79 dBm	375	mA
	LTE-FDD B66 CH66536 @ 23.01 dBm	770	mA
	LTE-FDD B71 CH68836 @ 22.72 dBm	697	mA

Table 50: EG060K-LA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.4	mA
	WCDMA PF = 64 (USB disconnected)	2.7	mA
	WCDMA PF = 128 (USB disconnected)	2.1	mA
	WCDMA PF = 512 (USB disconnected)	1.7	mA
	LTE-FDD PF = 32 (USB disconnected)	4.2	mA
	LTE-FDD PF = 64 (USB disconnected)	2.9	mA
	LTE-FDD PF = 128 (USB disconnected)	2.3	mA
	LTE-TDD PF = 32 (USB disconnected)	4.4	mA
	LTE-TDD PF = 64 (USB disconnected)	3.1	mA
	LTE-TDD PF = 128 (USB disconnected)	2.3	mA

Idle state	WCDMA PF = 64 (USB disconnected)	12	mA
	WCDMA PF = 64 (USB 2.0 connected)	20	mA
	LTE-FDD PF = 64 (USB disconnected)	12	mA
	LTE-FDD PF = 64 (USB 2.0 connected)	20	mA
	LTE-TDD PF = 64 (USB disconnected)	12	mA
	LTE-TDD PF = 64 (USB 2.0 connected)	20	mA
WCDMA data transfer (GNSS OFF)	WCDMA B2 HSDPA CH9537 @ 22.1 dBm	616	mA
	WCDMA B2 HSUPA CH9263 @ 21.38 dBm	551	mA
	WCDMA B4 HSDPA CH1313 @ 22.12 dBm	647	mA
	WCDMA B4 HSUPA CH1313 @ 20.34 dBm	491	mA
	WCDMA B5 HSDPA CH4232 @ 22.33 dBm	538	mA
	WCDMA B5 HSUPA CH4232 @ 22.58 dBm	549	mA
	WCDMA B8 HSDPA CH2862 @ 22.44 dBm	577	mA
	WCDMA B8 HSUPA CH2862 @ 22 dBm	554	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 CH900 @ 22.88 dBm	668	mA
	LTE-FDD B4 CH2175 @ 22.79 dBm	788	mA
	LTE-FDD B5 CH2525 @ 23.07 dBm	583	mA
	LTE-FDD B7 CH3100 @ 22.43 dBm	754	mA
	LTE-FDD B8 CH3625 @ 22.76 dBm	622	mA
	LTE-FDD B25 CH8365 @ 22.91 dBm	678	mA
	LTE-FDD B28 CH27460 @ 23.11 dBm	629	mA
	LTE-TDD B66 CH66786 @ 22.91 dBm	809	mA
	LTE-TDD B42 CH42590 @ 22.46 dBm	381	mA
	LTE-TDD B43 CH44590 @ 22.8 dBm	304	mA
WCDMA voice	WCDMA B2 CH9537 @ 23.15 dBm	667	mA

call	WCDMA B4 CH1313 @ 23.22 dBm	706	mA
	WCDMA B5 CH4232 @ 23.31 dBm	583	mA
	WCDMA B8 CH2862 @ 23.36 dBm	635	mA

Table 51: EG120K-LA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.4	mA
	WCDMA PF = 64 (USB disconnected)	2.7	mA
	WCDMA PF = 128 (USB disconnected)	2.1	mA
	WCDMA PF = 512 (USB disconnected)	1.7	mA
	LTE-FDD PF = 32 (USB disconnected)	4.2	mA
	LTE-FDD PF = 64 (USB disconnected)	3.4	mA
	LTE-FDD PF = 128 (USB disconnected)	1.9	mA
	LTE-TDD PF = 32 (USB disconnected)	4.4	mA
	LTE-TDD PF = 64 (USB disconnected)	3.1	mA
	LTE-TDD PF = 128 (USB disconnected)	2.3	mA
Idle state	WCDMA PF = 64 (USB disconnected)	12	mA
	WCDMA PF = 64 (USB 2.0 connected)	20	mA
	LTE-FDD PF = 64 (USB disconnected)	10.2	mA
	LTE-FDD PF = 64 (USB 2.0 connected)	20	mA
	LTE-TDD PF = 64 (USB disconnected)	12	mA
	LTE-TDD PF = 64 (USB 2.0 connected)	20	mA
WCDMA data transfer (GNSS OFF)	WCDMA B2 HSDPA CH9537 @ 22.11 dBm	602	mA
	WCDMA B2 HSUPA CH9263 @ 21.95 dBm	523	mA

	WCDMA B4 HSDPA CH1313 @ 22.12 dBm	613	mA
	WCDMA B4 HSUPA CH1450 @ 20.83 dBm	489	mA
	WCDMA B5 HSDPA CH4232 @ 22.4 dBm	539	mA
	WCDMA B5 HSUPA CH4232 @ 22.91 dBm	566	mA
	WCDMA B8 HSDPA CH2862 @ 22.44 dBm	571	mA
	WCDMA B8 HSUPA CH2862 @ 22.15 dBm	555	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 CH900 @ 22.88 dBm	666	mA
	LTE-FDD B4 CH2175 @ 22.85 dBm	674	mA
	LTE-FDD B5 CH2525 @ 23.04 dBm	583	mA
	LTE-FDD B7 CH3100 @ 22.64 dBm	775	mA
	LTE-FDD B8 CH3625 @ 22.92 dBm	625	mA
	LTE-FDD B25 CH8365 @ 22.98 dBm	678	mA
	LTE-FDD B28 CH27460 @ 22.89 dBm	636	mA
	LTE-TDD B66 CH66786 @ 23 dBm	720	mA
	LTE-TDD B42 CH42590 @ 22.64 dBm	386	mA
	LTE-TDD B43 CH44590 @ 22.71 dBm	311	mA
WCDMA voice call	WCDMA B2 CH9537 @ 23.1 dBm	648	mA
	WCDMA B4 CH1313 @ 23.21 dBm	664	mA
	WCDMA B5 CH4232 @ 23.37 dBm	584	mA
	WCDMA B8 CH2862 @ 23.3 dBm	627	mA

6.4. Digital I/O Characteristics

Table 52: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × VDD_EXT	VDD_EXT + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.3 × VDD_EXT	V
V_{OH}	High-level output voltage	VDD_EXT - 0.45	VDD_EXT	V
V_{OL}	Low-level output voltage	0	0.45	V

Table 53: USIM_VDD 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 54: USIM_VDD 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 55: SDIO_VDD 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.27	2.0	V
V_{IL}	Low-level input voltage	-0.3	0.58	V
V_{OH}	High-level output voltage	1.4	SDIO_VDD	V
V_{OL}	Low-level output voltage	0	0.45	V

Table 56: SDIO_VDD 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.625 × SDIO_VDD	SDIO_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.25 × SDIO_VDD	V
V_{OH}	High-level output voltage	0.75 × SDIO_VDD	SDIO_VDD	V
V_{OL}	Low-level output voltage	0	0.125× SDIO_VDD	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 57: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operation and Storage Temperatures

Table 58: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [11]	-30	+25	+75	ºC
Extended Operation Range [12]	-40	-	+85	ºC
Storage temperature range	-40	-	+90	ºC

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;

[11] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications.
[12] To meet this extended temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, emergency call*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

- Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

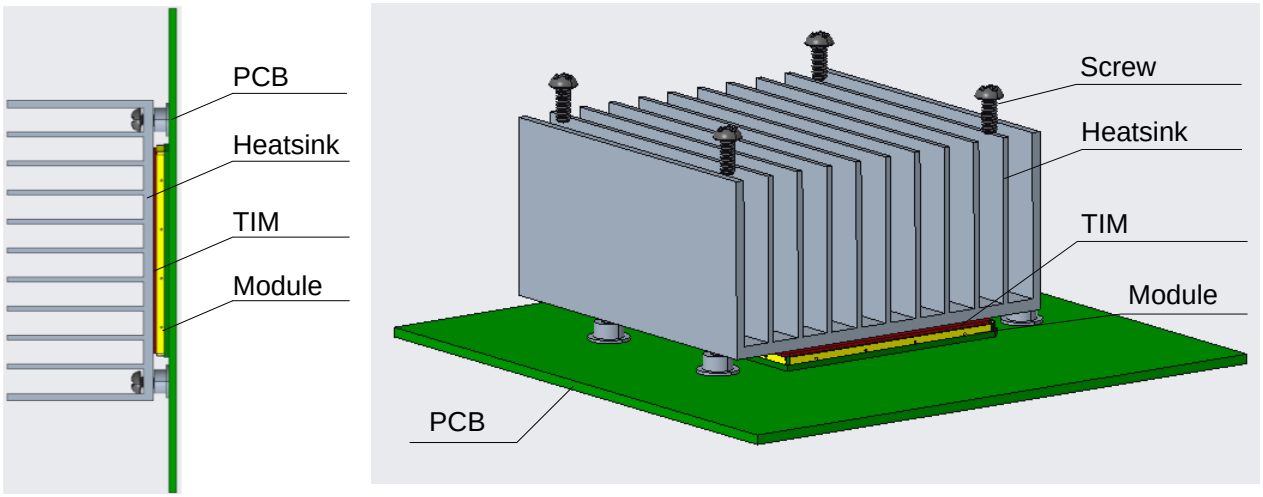


Figure 41: Placement and Fixing of the Heatsink

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

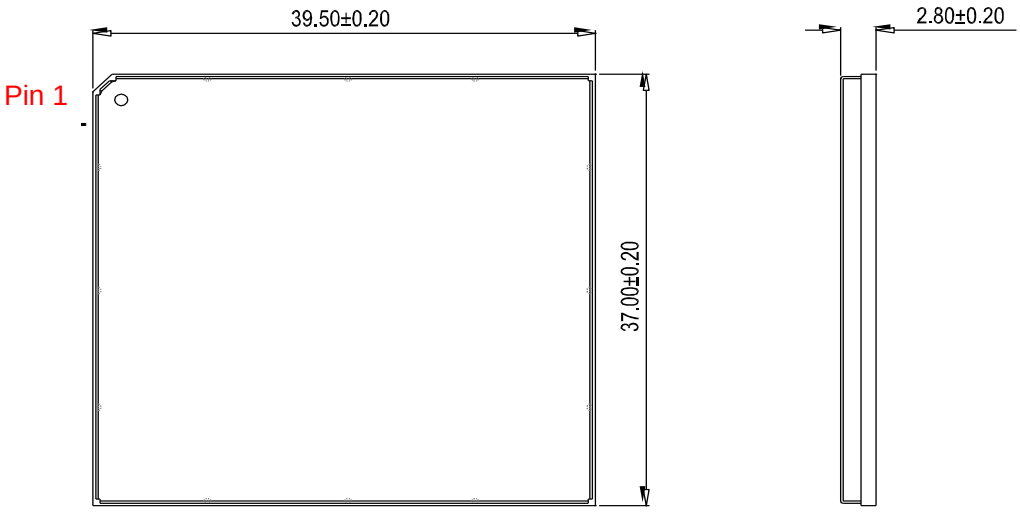


Figure 42: Module Top and Side Dimensions

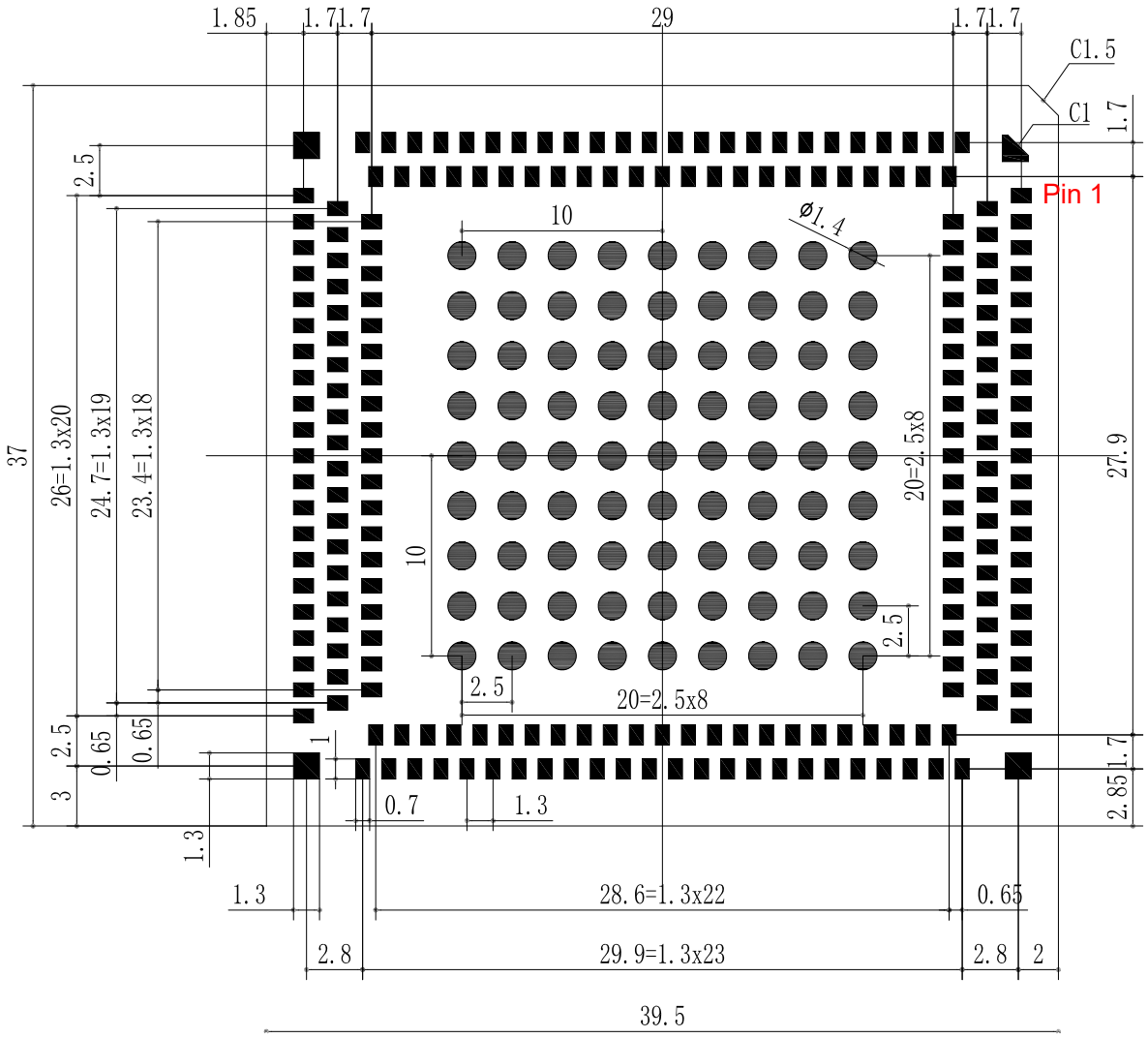


Figure 43: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

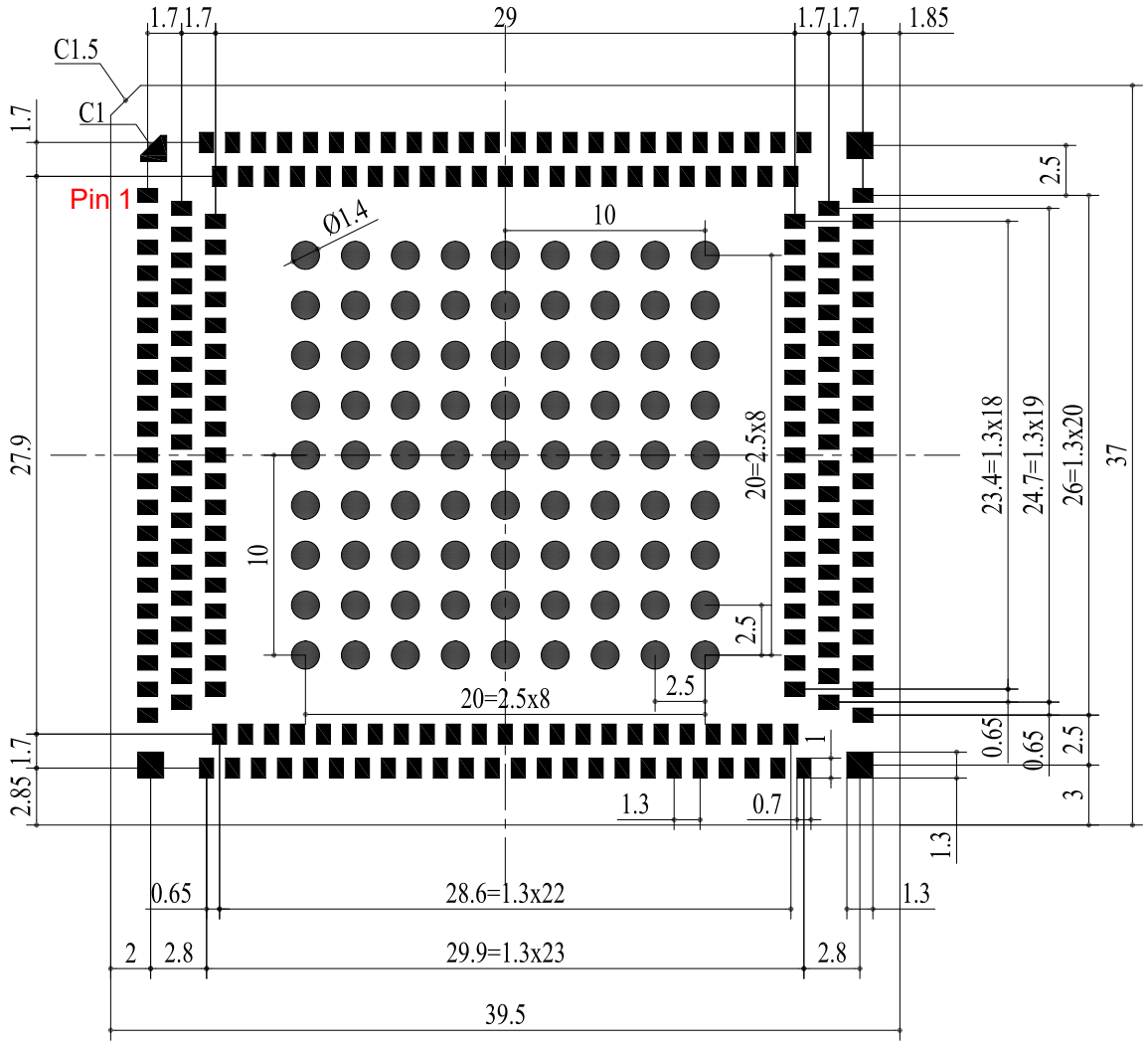


Figure 44: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

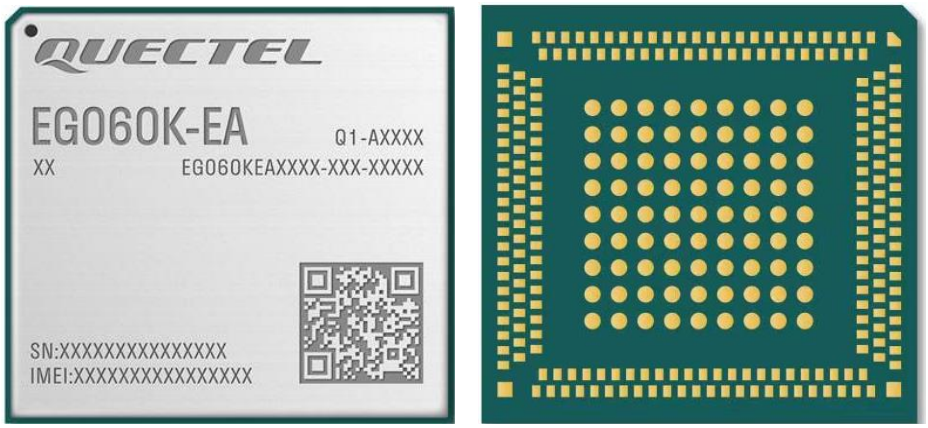


Figure 45: Top and Bottom Views of EG060K-EA

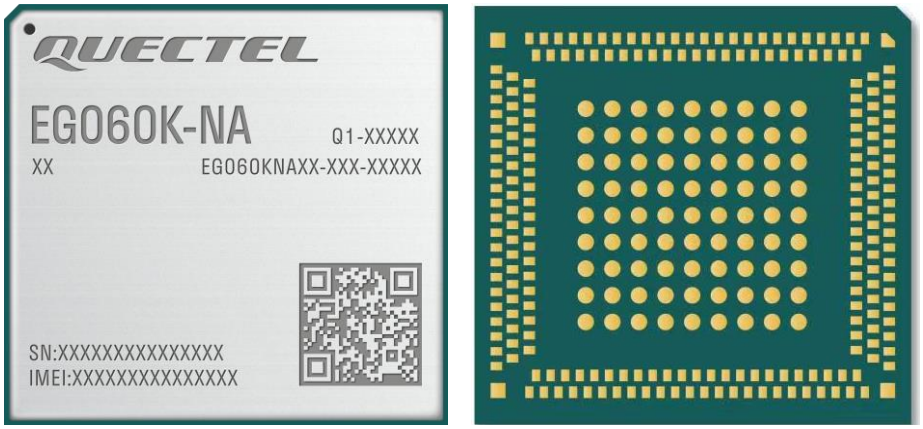


Figure 46: Top and Bottom Views of EG060K-NA

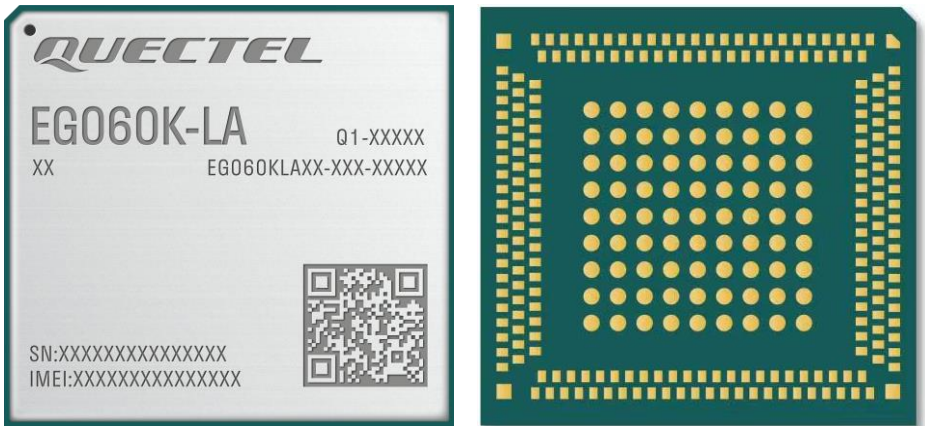


Figure 47: Top and Bottom Views of EG060K-LA

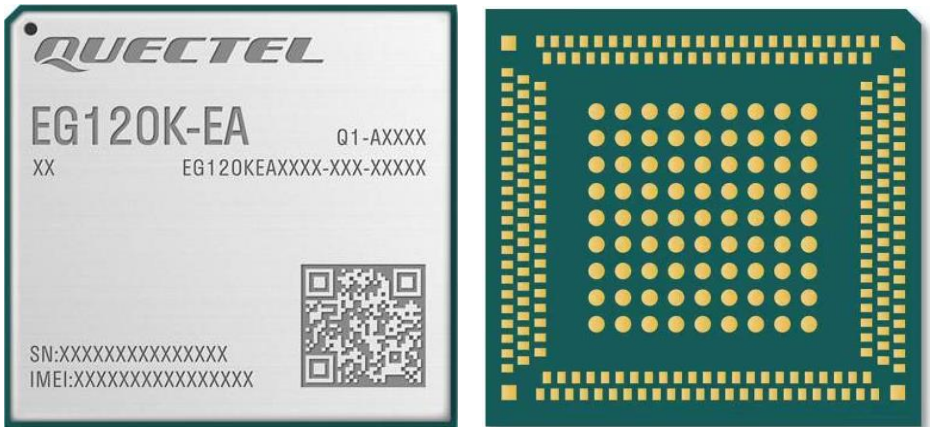


Figure 48: Top and Bottom Views of EG120K-EA

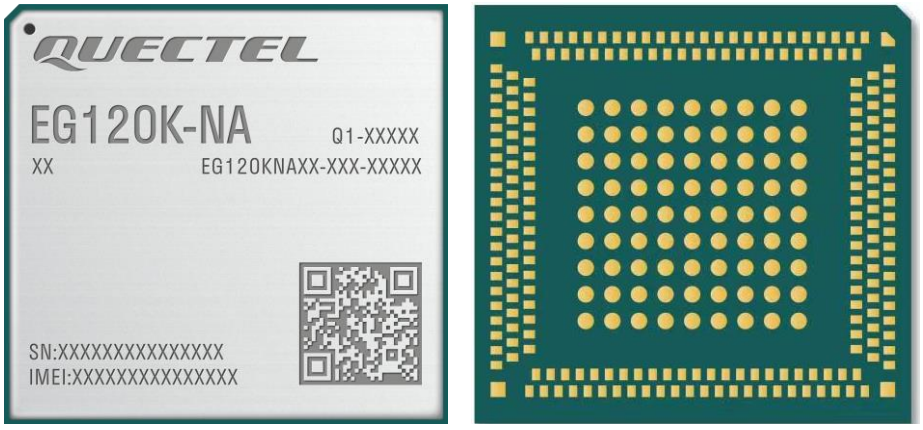


Figure 49: Top and Bottom Views of EG120K-NA

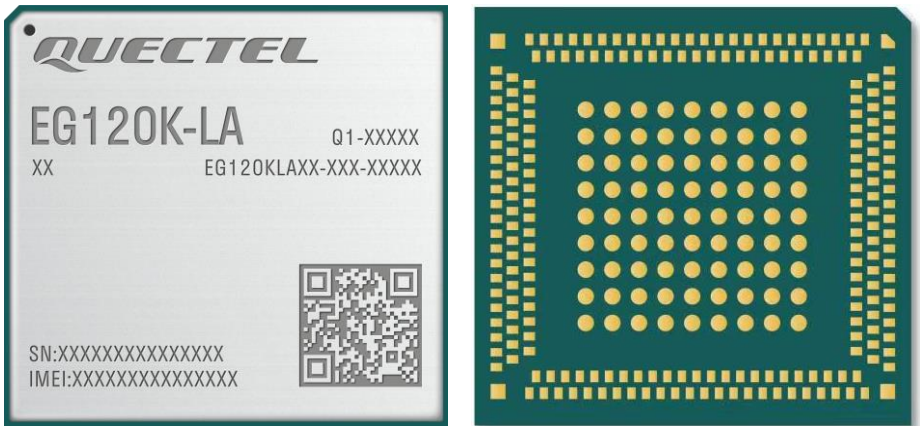


Figure 50: Top and Bottom Views of EG120K-LA

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, see the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [13] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[13] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see IPC/JEDEC J-STD-033 for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.18 mm. For more details, see ***document [6]***

The peak reflow temperature ranges from 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

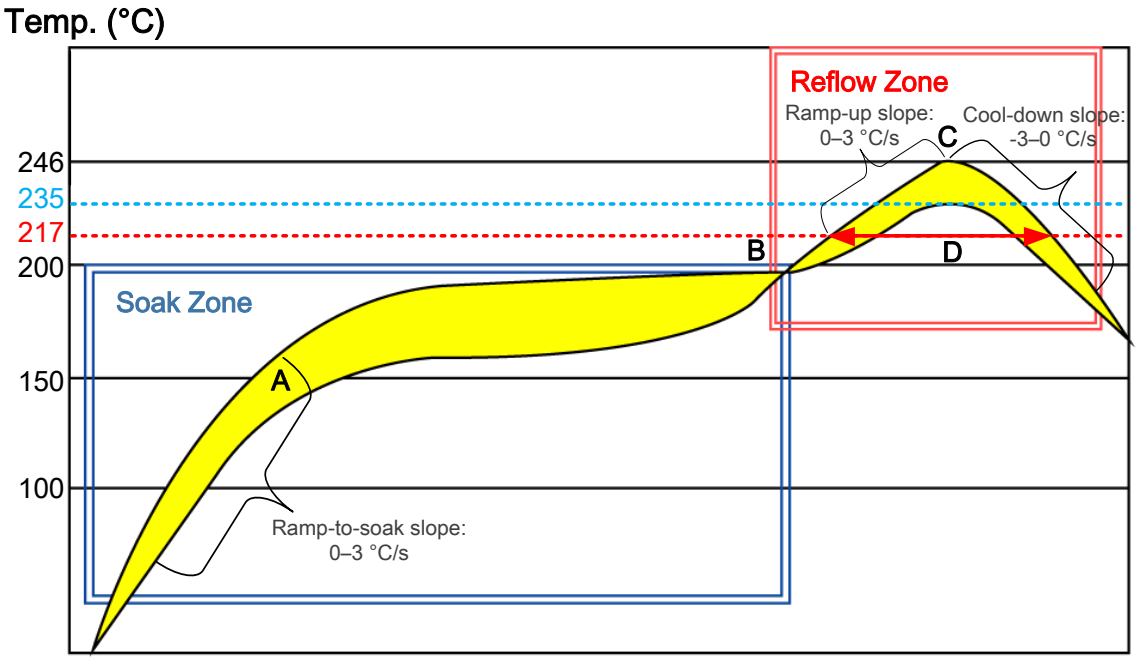


Figure 51: Reflow Soldering Thermal Profile

Table 59: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

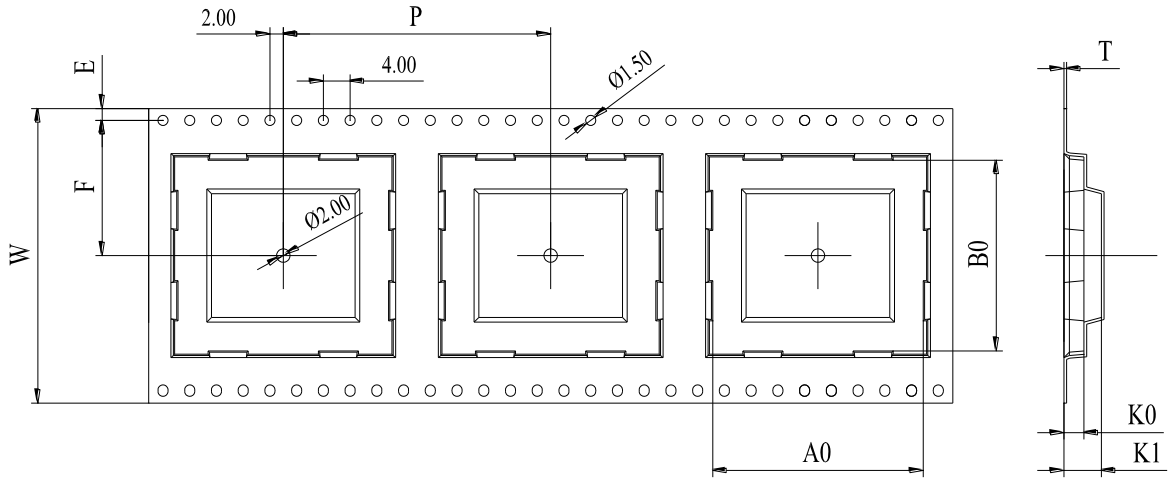


Figure 52: Carrier Tape Dimension Drawing

Table 60: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
56	48	0.35	40	37.5	3.9	5.3	26.2	1.75

8.3.2. Plastic Reel

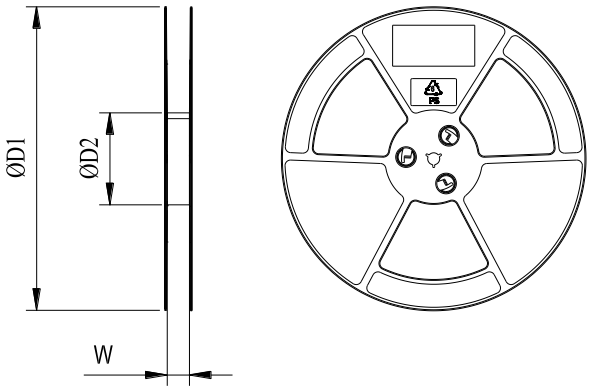


Figure 53: Plastic Reel Dimension Drawing

Table 61: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	56.5

8.3.3. Mounting Direction

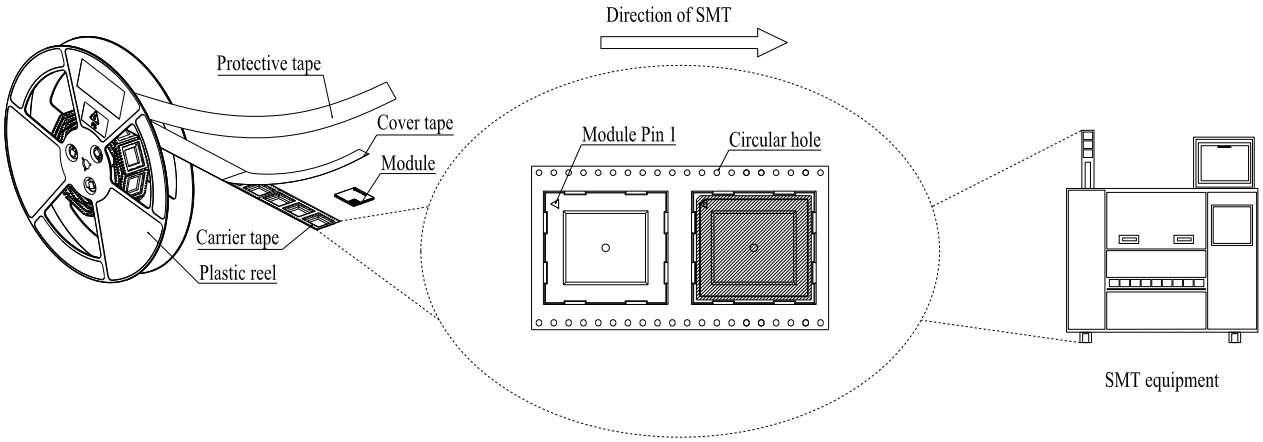
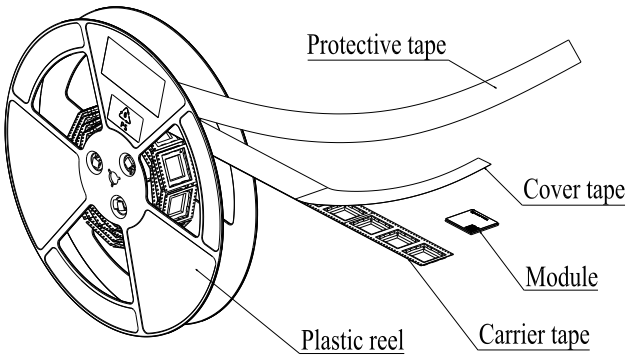


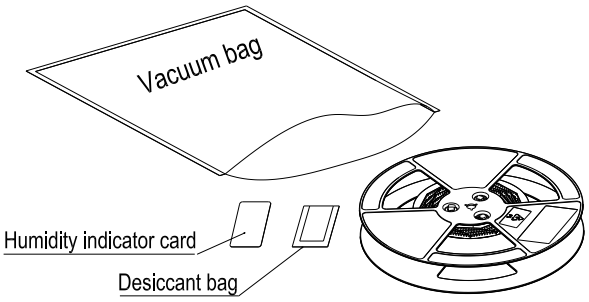
Figure 54: Mounting Direction

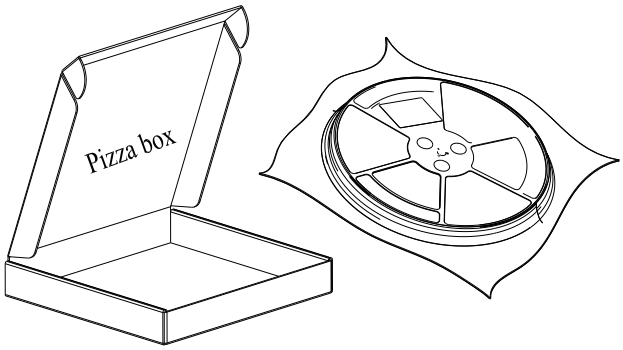
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 200 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 800 modules.

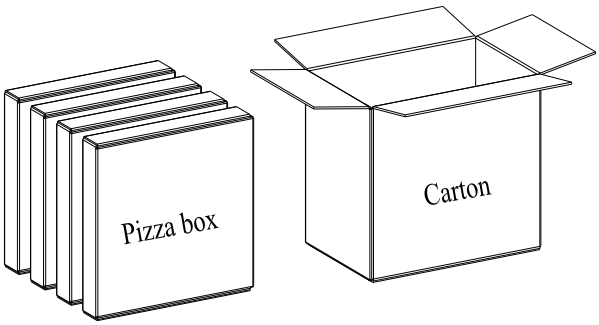


Figure 55: Packaging Process

9 Appendix References

Table 62: Related Documents

Document Name
[1] Quectel_EG060K_Series_CA_Feature
[2] Quectel_EG120K_Series_CA_Feature
[3] Quectel_UMTS&LTE_EVB_R2.0_User_Guide
[4] Quectel_EG06xK&Ex120K&EM060K_Series_AT_Commands_Manual
[5] Quectel_RF_Layout_Application_Note
[6] Quectel_Module_Secondary_SMT_Application_Note

Table 63: Term and Abbreviation

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
AMR-WB	Adaptive Multi-Rate Wideband
BDS	BeiDou Navigation Satellite System
bps	bit(s) per second
CA	Carrier Aggregation
CHAP	Challenge-Handshake Authentication Protocol
CPE	Customer Premise Equipment
CS	Coding Scheme

CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DFOTA	Delta Firmware Upgrade Over-the-Air
DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVB	Evaluation Board
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GND	Ground
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HSPA+	Evolved High Speed Packet Access
I/O	Input/Output
LDO	Low-dropout Regulator
LED	Light Emitting Diode

LGA	Land Grid Array
LNA	Low-Noise Amplifier
LTE	Long-Term Evolution
M2M	Machine to Machine
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	Mobile Station
MT	Mobile Terminated
NAND	NON-AND
NMEA	National Marine Electronics Association
OTG	On-The-Go
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
POS	Point of Sale
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RTS	Ready To Send/Request to Send

RF	Radio Frequency
RHCP	Right Hand Circular Polarization
Rx	Receive
SD Card	Secure Digital Card
SDIO	Secure Digital Input/Output
SIMO	Single Input Multiple Output
SPI	Serial Peripheral Interface
SIMO	Single Input Multiple Output
SLIC	Subscriber Line Interface Circuit
SMD	Surface Mount Device
SMS	Short Message Service
SMT	Surface Mount Technology
TCP	Transmission Control Protocol
TDD	Time Division Duplex
TIM	Thermal Interface Material
TTFF	Time to First Fix
TVS	Transient Voltage Suppressor
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery

Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access