EC200A Series

Reference Design

LTE Standard Module Series

Version: 1.0

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2021-11-26	Anthony LIU	Creation of the document
1.0	2022-02-15	Anthony LIU	First official release

Contents

1 Reference Design

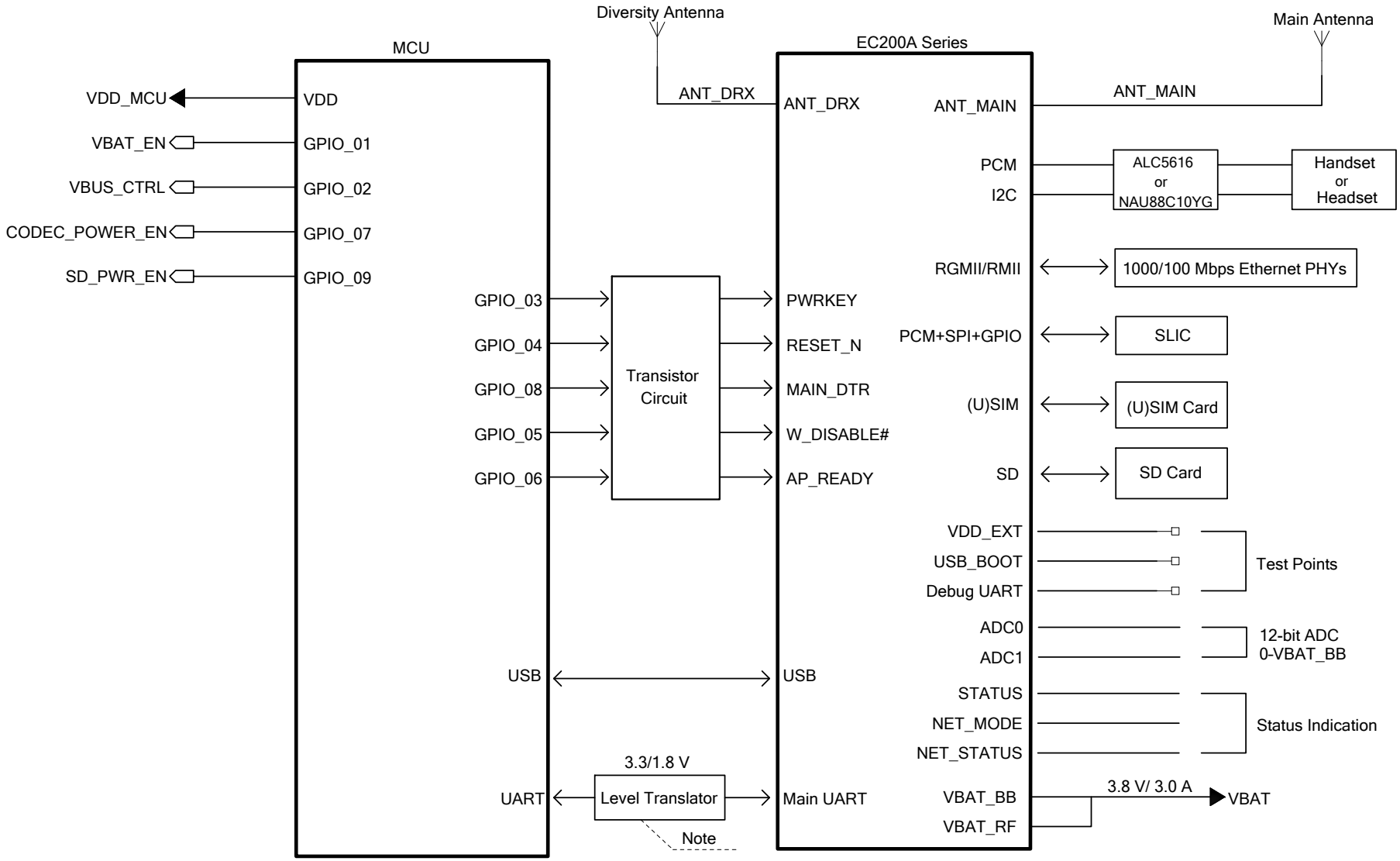
1.1. Introduction

This document provides the reference design of Quectel EC200A series module, including block diagrams of power supply and module design, analog audio, (U)SIM, RGMII/RMII, SD card interfaces, etc.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Reference Design Block Diagram



NOTE:

A level-shifting circuit with triode or a level translator TXS0108EPWR provided by Texas Instruments is recommended.

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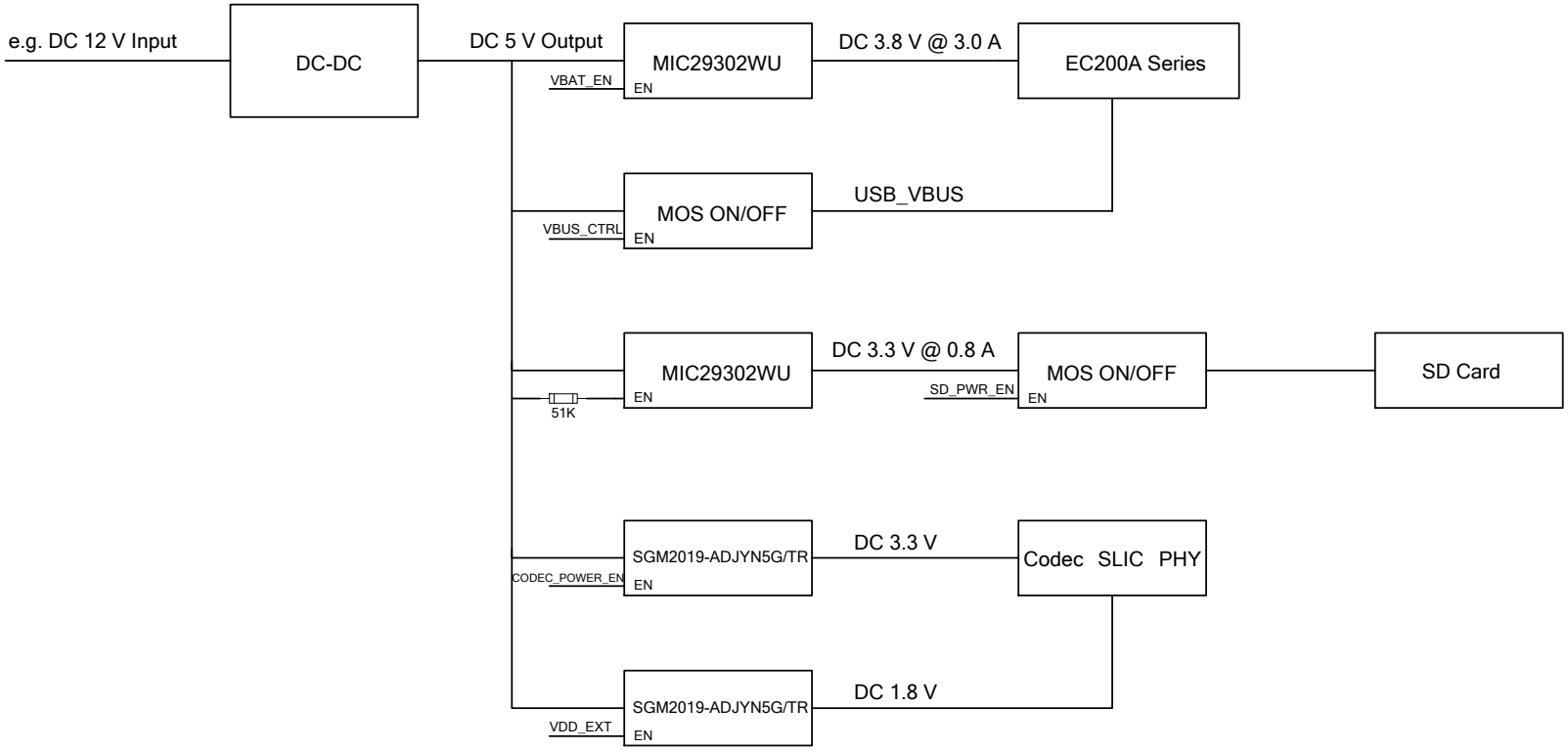
Power Supply Block Diagram



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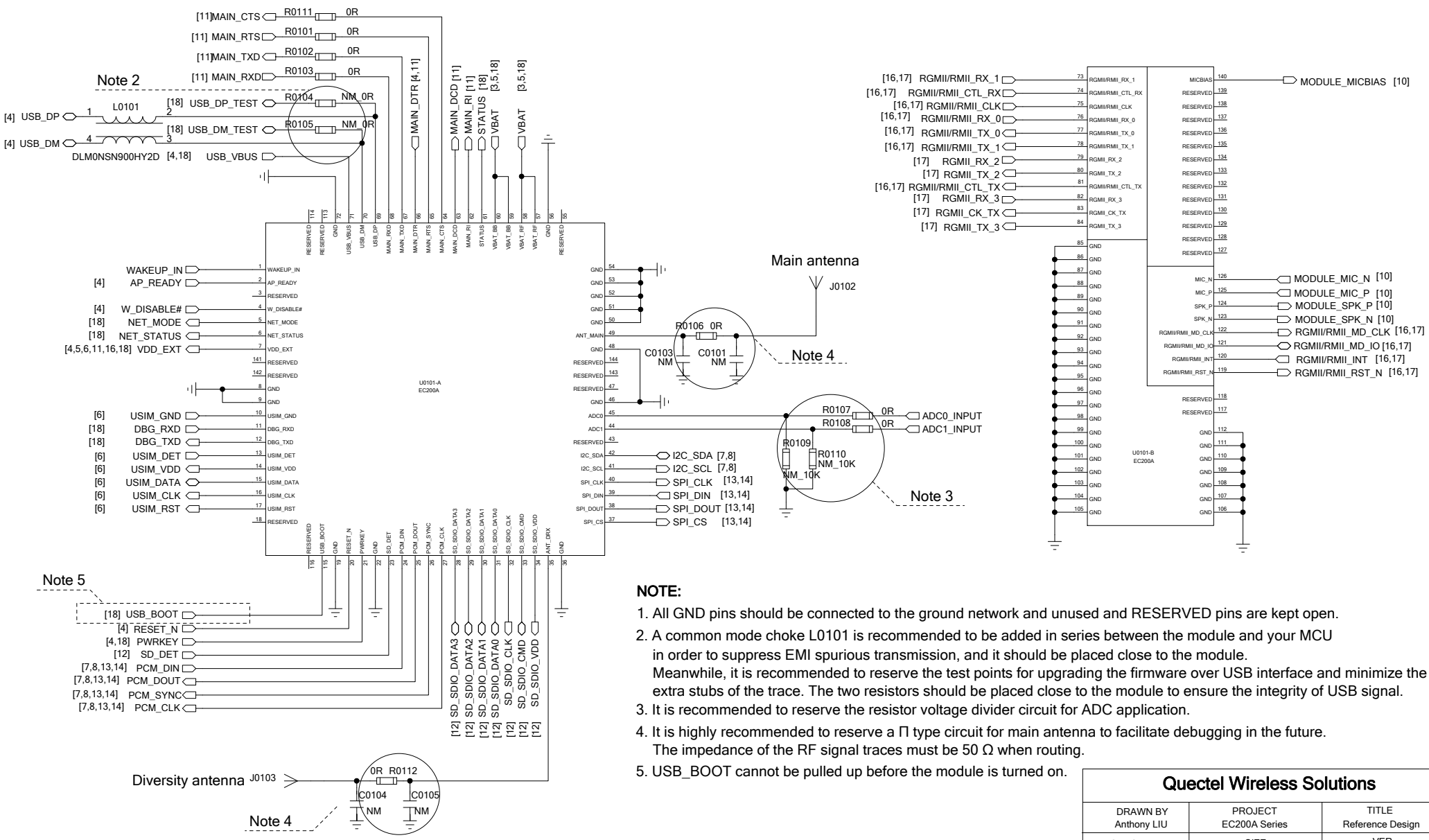
Module Interface



NOTE:

1. All GND pins should be connected to the ground network and unused and RESERVED pins are kept open.
2. A common mode choke L0101 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission, and it should be placed close to the module. Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. The two resistors should be placed close to the module to ensure the integrity of USB signal.
3. It is recommended to reserve the resistor voltage divider circuit for ADC application.
4. It is highly recommended to reserve a Π type circuit for main antenna to facilitate debugging in the future. The impedance of the RF signal traces must be 50 Ω when routing.
5. USB_BOOT cannot be pulled up before the module is turned on.

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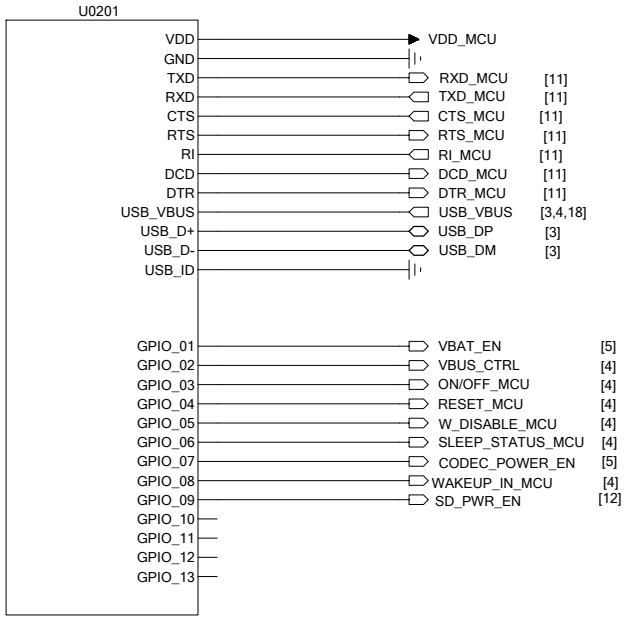
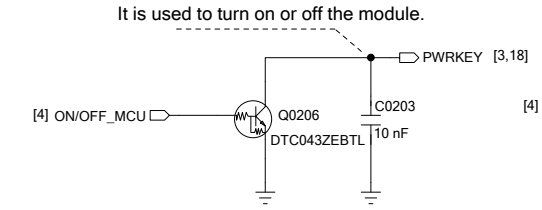
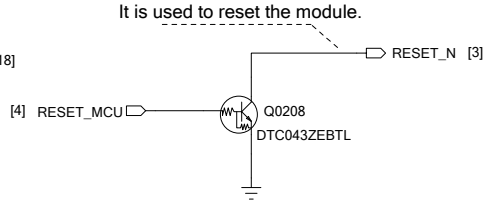
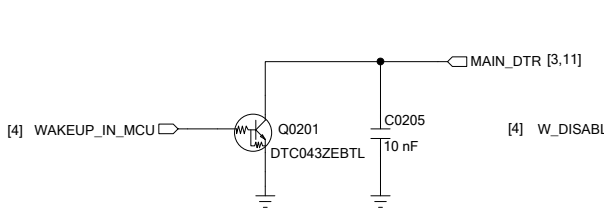
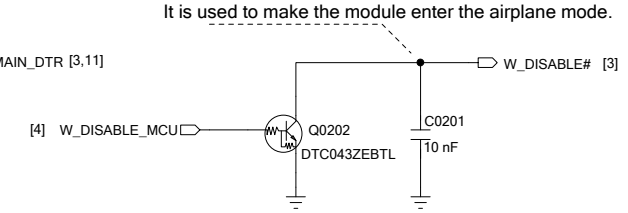
MCU Interface

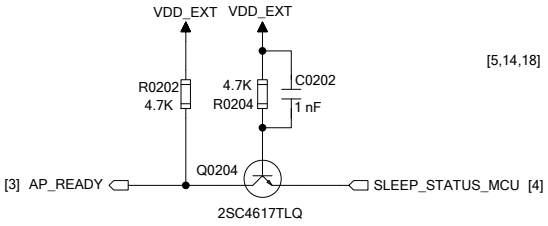


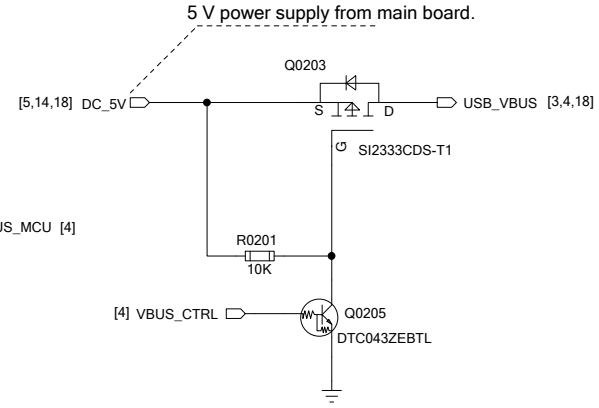












NOTE:

1. U0201 represents your MCU. The power domain of GPIO interfaces of EC200A series is 1.8 V.
   If the GPIO interfaces of U0201 is also 1.8 V, then the related level-shifting circuit is not needed.
2. It is recommended to select GPIO pins which are at low level by default as the control pins for PWRKEY and RESET_N of the module.
   Ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.

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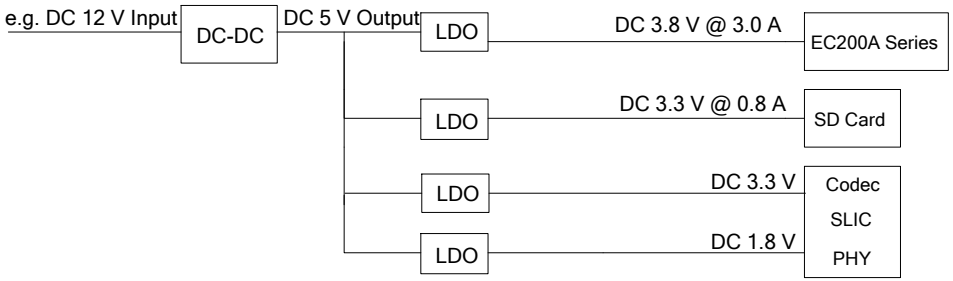
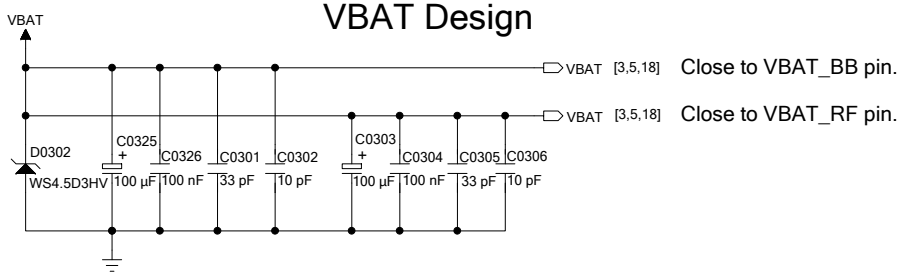
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the input voltage into a 5.0 V output, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V.



VBAT Design

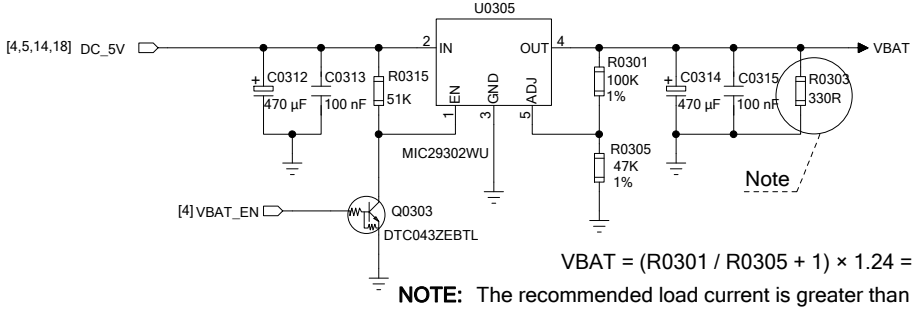


NOTE:

1. The VBAT supply current must meet the rated output capacity of 3.0 A.
2. VBAT should be routed in star configuration to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.4-4.5 V.

LDO Application

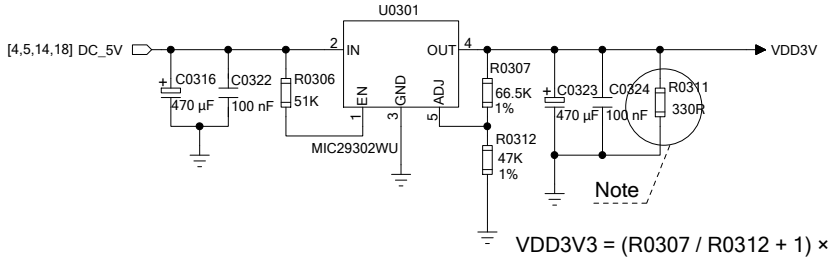
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



VBAT = (R0301 / R0305 + 1) × 1.24 = 3.88 V

NOTE: The recommended load current is greater than 10 mA.

Power Supply for SD Card

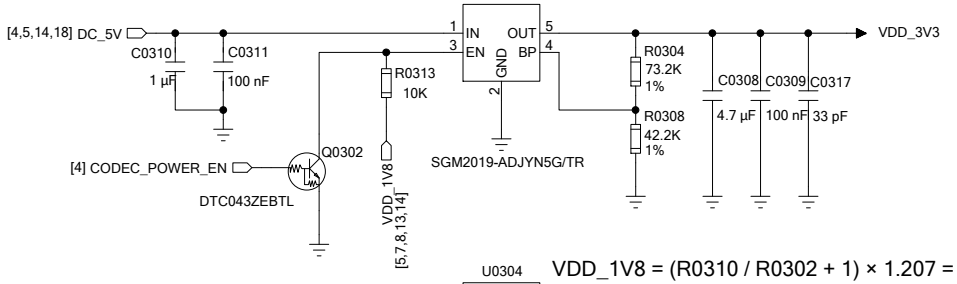


VDD3V3 = (R0307 / R0312 + 1) × 1.24 = 3 V

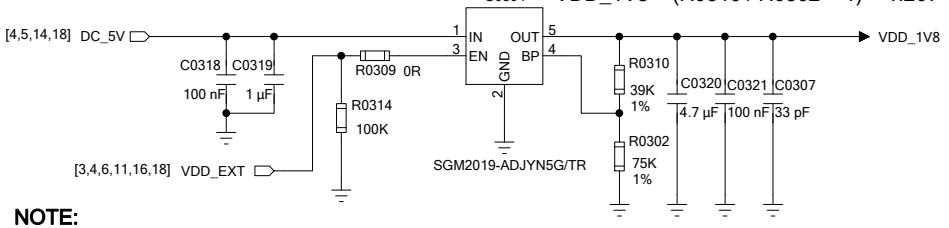
NOTE: The recommended load current is greater than 10 mA.

Power Supply for PCM Codec&SLIC&PHY

VDD_3V3 = (R0304 / R0308 + 1) × 1.207 = 3.3 V



VDD_1V8 = (R0310 / R0302 + 1) × 1.207 = 1.8 V



NOTE:

1. CODEC_POWER_EN must be at a low level in order to ensure the normal output voltage of VDD_3V3. If VDD_3V3 power supply needs to be switched off, please keep CODEC_POWER_EN at high level.
2. The following power-up/down sequences should be followed to ensure the audio codec works normally.

   Power-up sequence: power up VDD_1V8 first, then VDD_3V3.
   Power-down sequence: power down VDD_3V3 first, then VDD_1V8.

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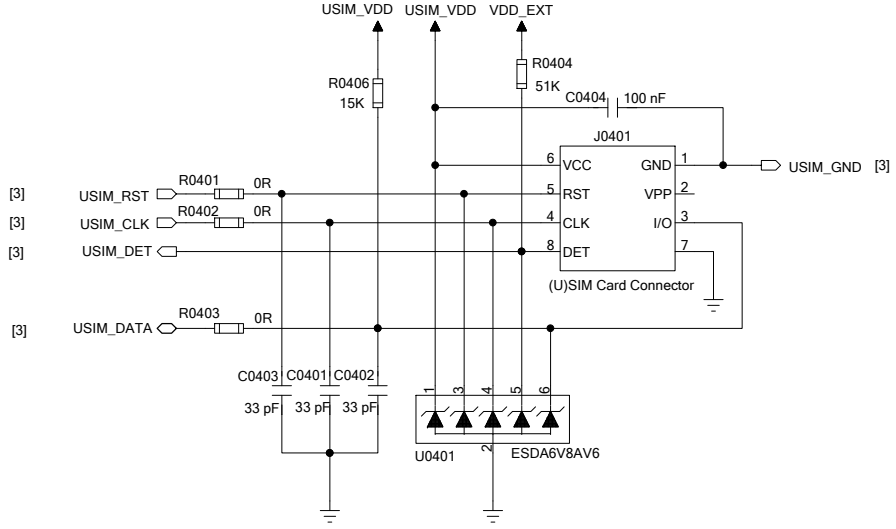
(U)SIM Interface Design



NOTE:

1. U0401 is recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The GND of the (U)SIM card connector is recommended to be connected to the module's USIM_GND. In addition, USIM_GND can also be connected to the GND of your PCB directly if the PCB's GND is complete.
3. The pull-up resistor R0406 of USIM_DATA can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
4. Connect 0 Ω resistors R0401-R0403 in series between the module and (U)SIM card for debugging; Capacitors C0401-C0403 can be used to filter out EGSM900 interference.
5. C0404's capacitance should be less than 1 μF and it should be placed close to the (U)SIM card connector.
6. For more information about the layout of (U)SIM interface, please refer to *Quectel_EC200A_Series_Hardware_Design*.

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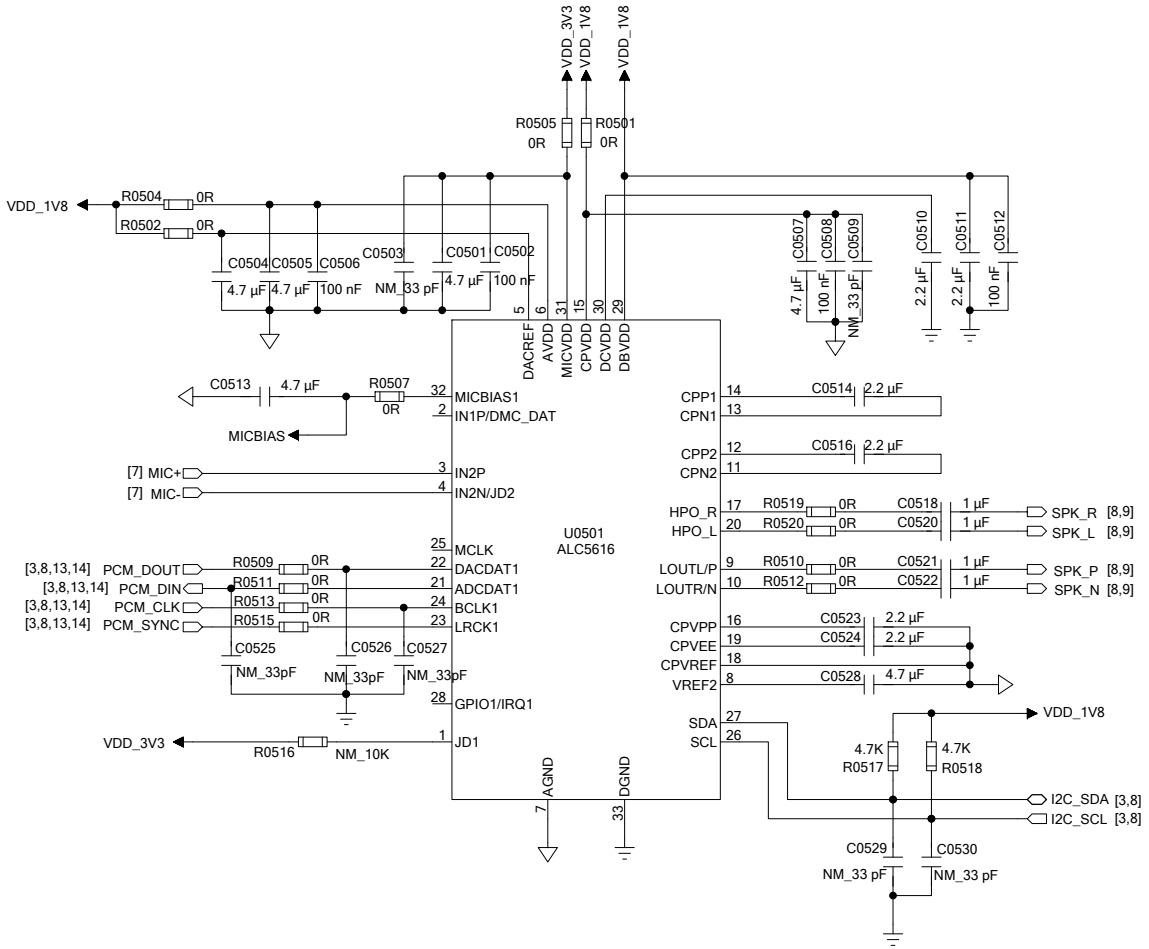
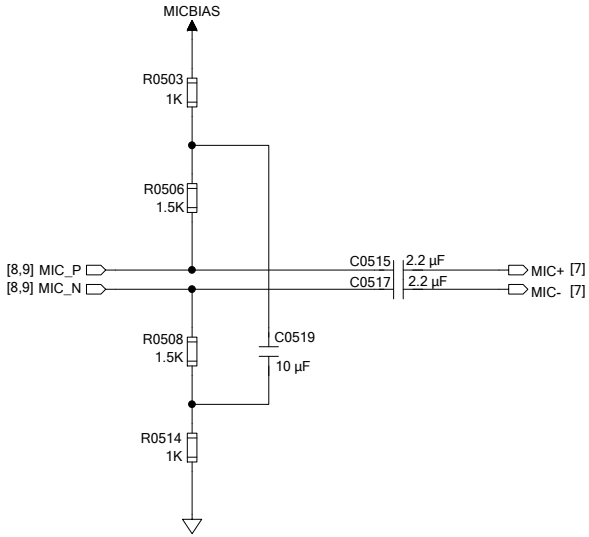
Audio Codec Design (ALC5616)





NOTE:

1. ALC5616 power-up sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD → MICVDD → software initialization.
2. ALC5616 power-down sequence: disable codec function by software → MICVDD → DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. The module will automatically initialize the codec via I2C interface after being turned on successfully, so all power supplies for the codec need to be powered on before that.
4. The analog ground and digital ground need to be connected with a 0 Ω resistor R-0805. For more details, please refer to sheet “Audio Codec Design (Analog Interfaces)”.
5. For more details, please refer to the datasheet of ALC5616.

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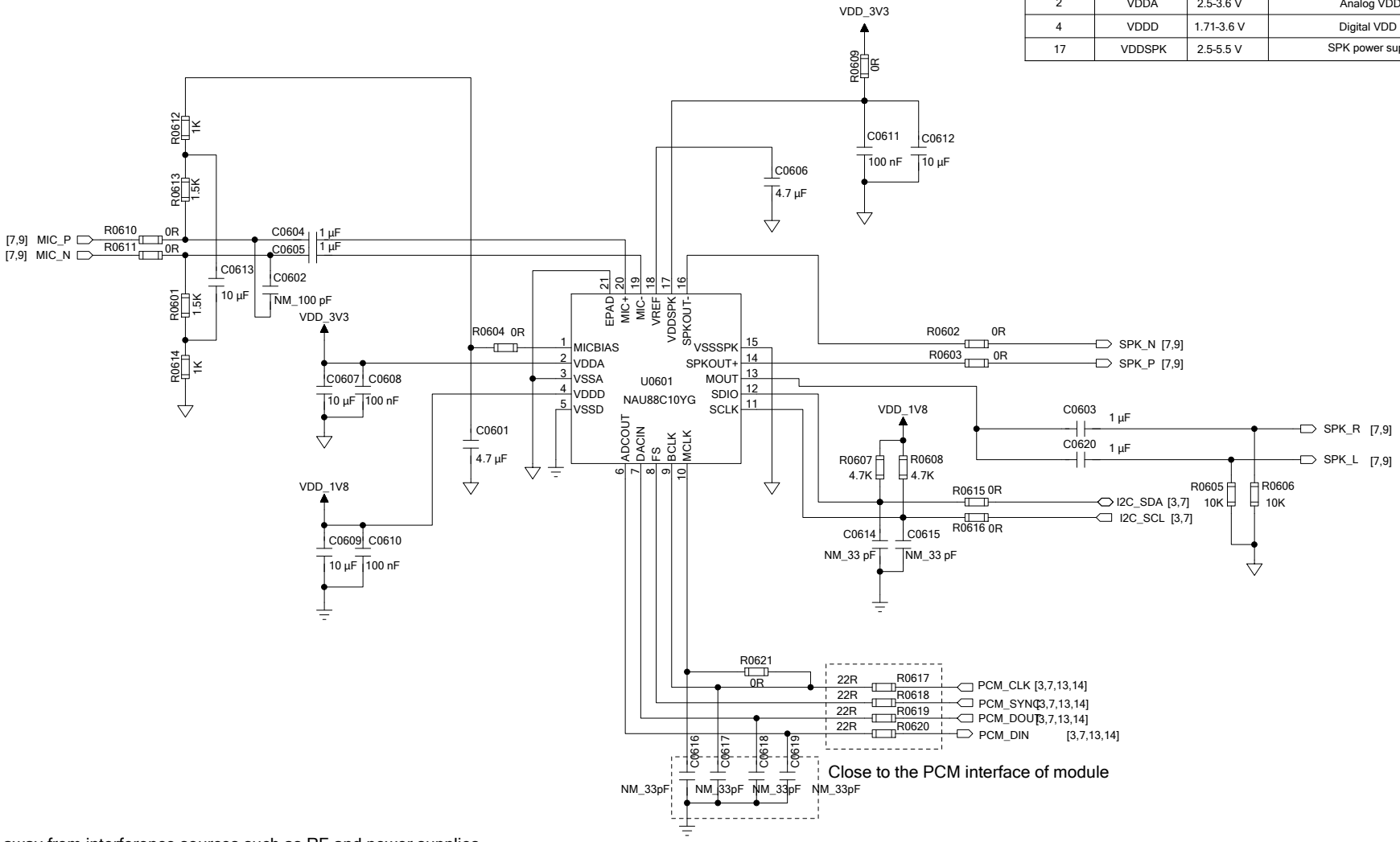
Audio Codec Design (NAU88C10YG)

Pin No.	Pin Name	Voltage	Description
2	VDDA	2.5-3.6 V	Analog VDD
4	VDDD	1.71-3.6 V	Digital VDD
17	VDDSPK	2.5-5.5 V	SPK power supply



NOTE:

1. The codec should be away from interference sources such as RF and power supplies, and the codec audio signal should be surrounded with ground as much as possible.
2. The voltage of VDDA pin must always be larger than that of VDDD.
3. The analog ground and digital ground need to be connected with a 0 Ω resistor R-0805. For more details, please refer to sheet “Audio Codec Design (Analog Interfaces)”.
4. For more details, please refer to the datasheet of NAU88C10YG.

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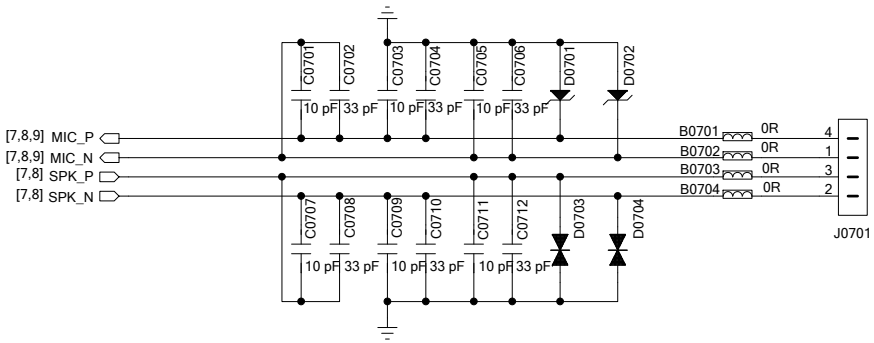
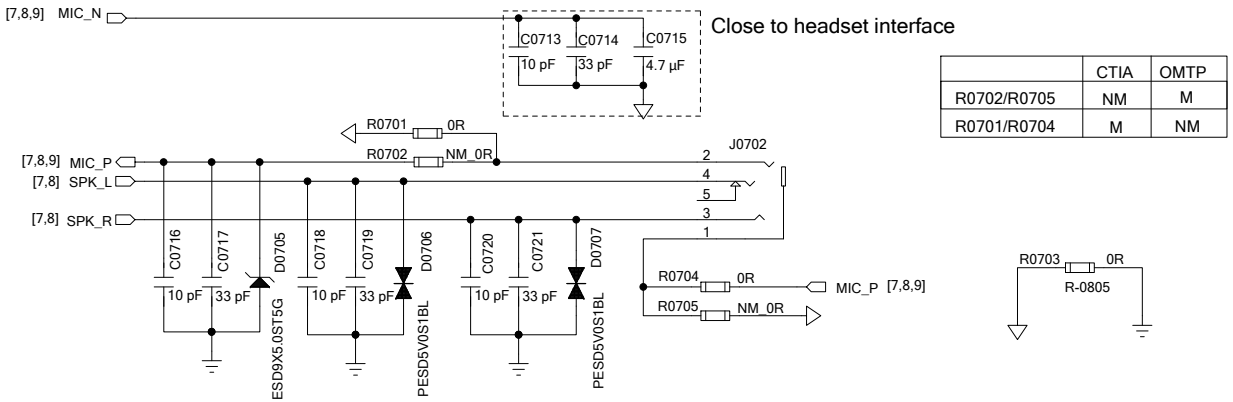
Audio Codec Design (Analog Interfaces)

Handset Application



Headset Application



	CTIA	OMTP
R0702/R0705	NM	M
R0701/R0704	M	NM

NOTE:

1. The analog output only drives handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset application, both the MIC and SPK signal traces need to be routed as differential pairs.
3. In headset application, the MIC signal traces need to be routed as a differential pair.
4. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals, etc.
5. You can choose either ALC5616 or NAU88C10YG in audio codec design.

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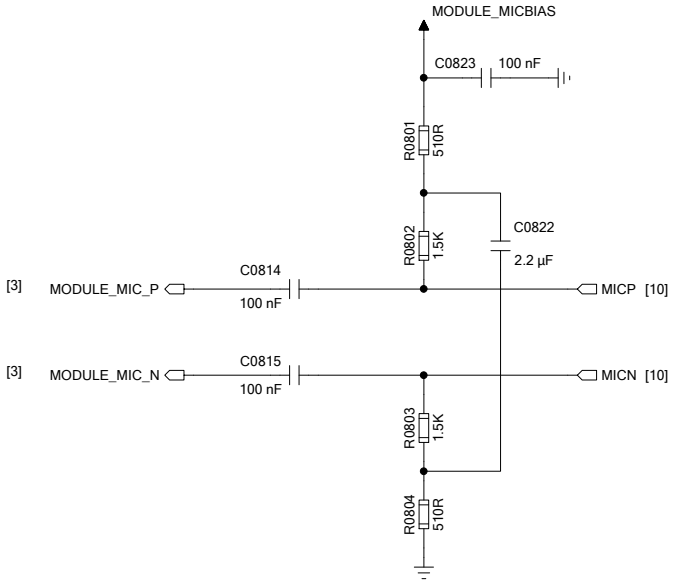
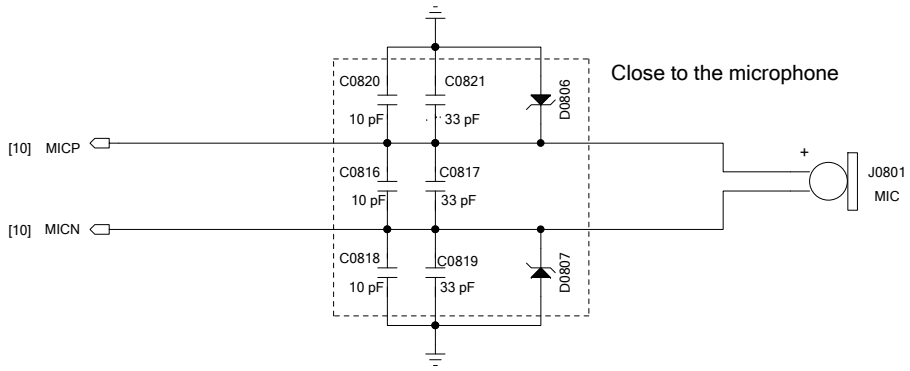
Module Analog Audio Interface Design

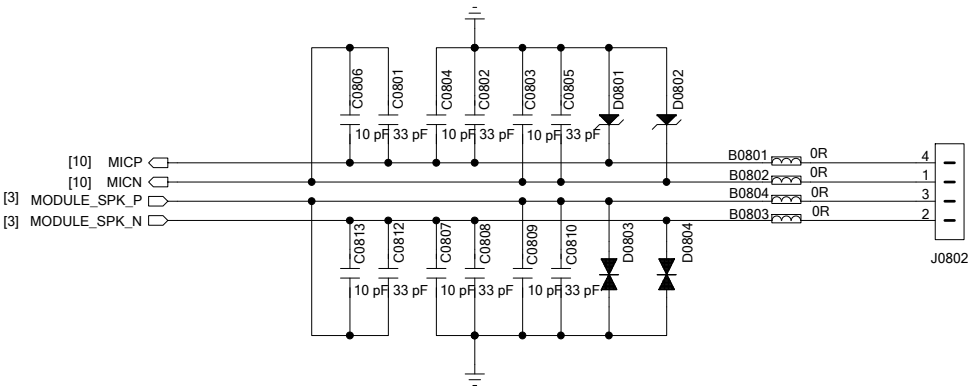
Microphone Bias Circuit



Microphone Application



Handset Application



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground.
3. In the audio design, you can choose either the analog audio or the codec.
4. The analog output only drives handset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.

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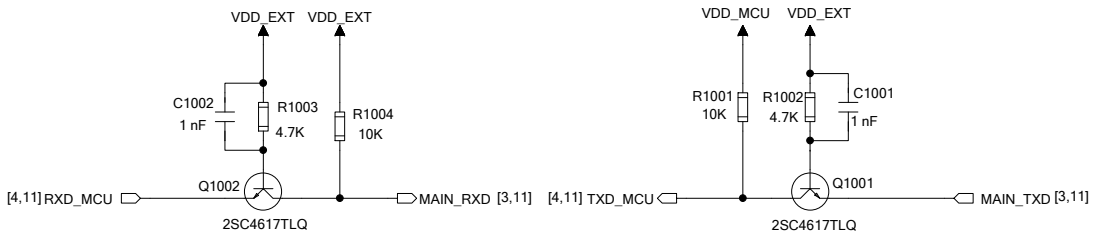
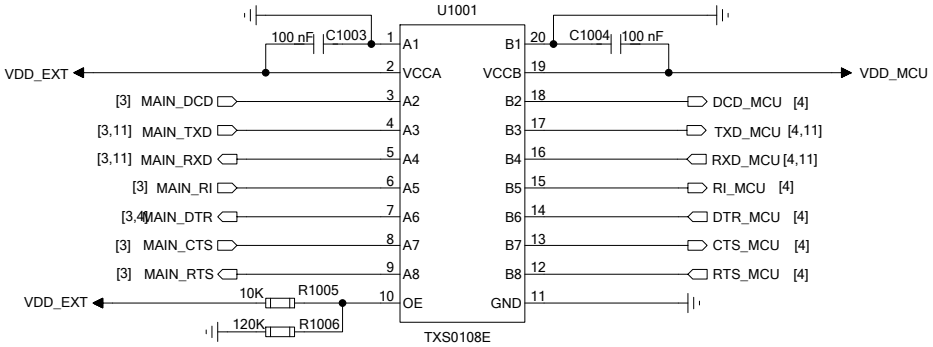
UART Interface Design

UART Level Conversion - Triode Solution



UART Level Conversion - IC Solution



NOTE:

1. There are two level conversion solutions: triode solution and IC solution, and the latter of which is recommended.
2. The power supply of TXS0108E's VCCA should not exceed that of VCCB.
   For more information, please refer to the datasheet from TI.
3. The transistor solution is not applicable for applications with baud rates exceeding 460 kbps.
   Capacitors C1001 and C1002 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR transistor circuits are similar to that of the MAIN_RXD interface.
   MAIN_CTS, MAIN_RI and MAIN_DCD transistor circuits are similar to that of the MAIN_TXD interface.

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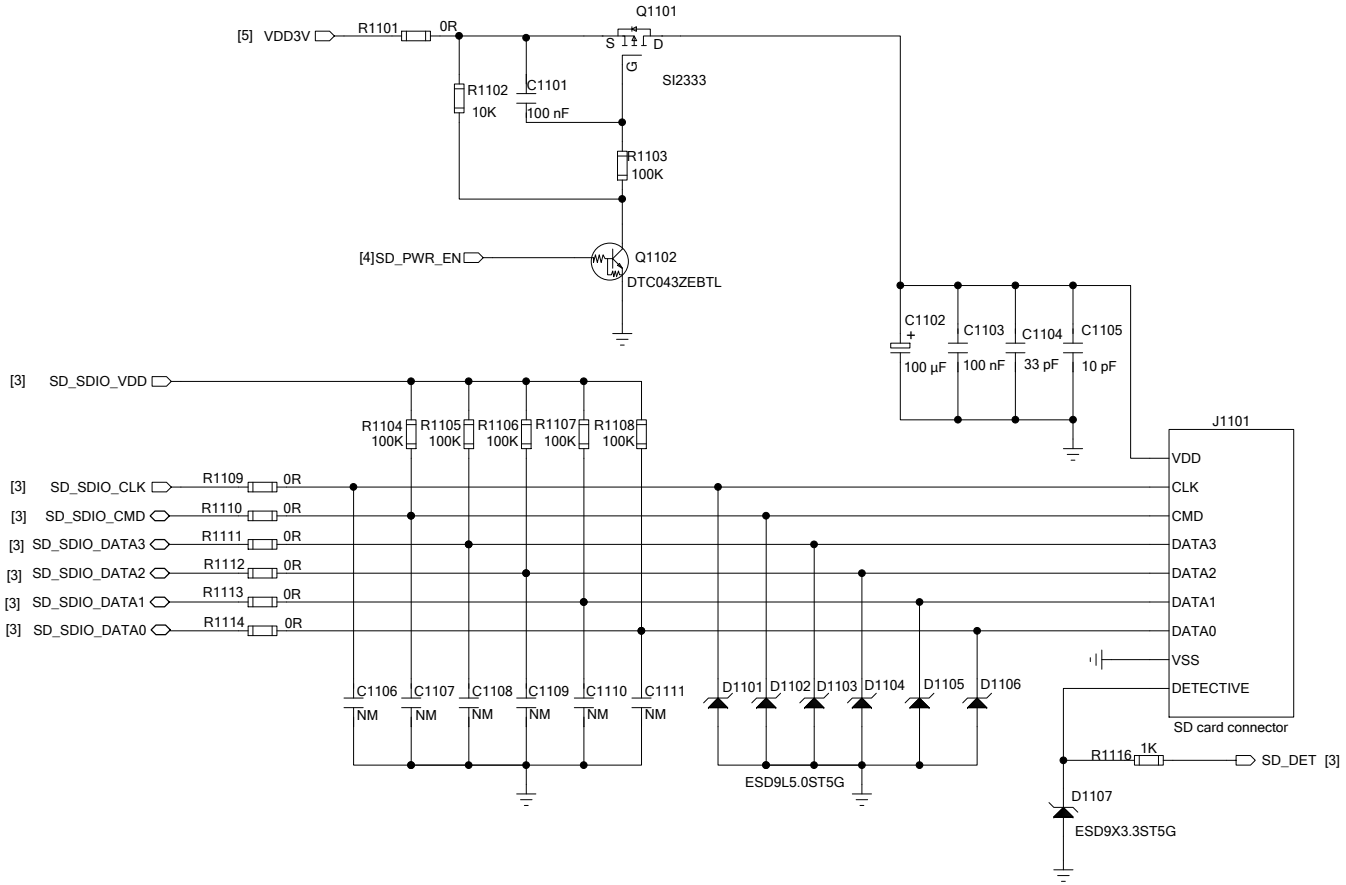
SD Card Interface Design



NOTE:

1. The pin 34 (SD_SDIO_VDD) on the module can only be used for the pull-up resistor of SDIO bus and its maximum output current is 50 mA.
2. The supply voltage range of VDD for SD card is 2.7-3.6 V and a sufficient current up to 0.8 A should be provided.
3. To avoid the jitter of bus, pull-up resistors R1104-R1108 are recommended to be added to SDIO bus. SD_SDIO_VDD should be used as the pull-up power. The values of these resistors are among 10-100 kΩ and the recommended value is 100 kΩ.
4. In order to improve the signal quality, it is recommended to add 0 Ω resistors R1109-R1114 in series between the module and the SD card connector. The bypass capacitors C1106-C1111 are reserved and not mounted by default.
5. In order to offer good ESD protection, it is recommended to add TVS diodes on SD card pins near the SD card connector with junction capacitance less than 15 pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
7. It is important to route SDIO signals with 50 Ω ±10 % impedance surrounded with ground on the layer and ground planes above and below and the total trace length should be less than 50 mm.
8. It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA [0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.
9. Make sure the adjacent trace spacing is two times the trace width and the bus capacitance is less than 15 pF.

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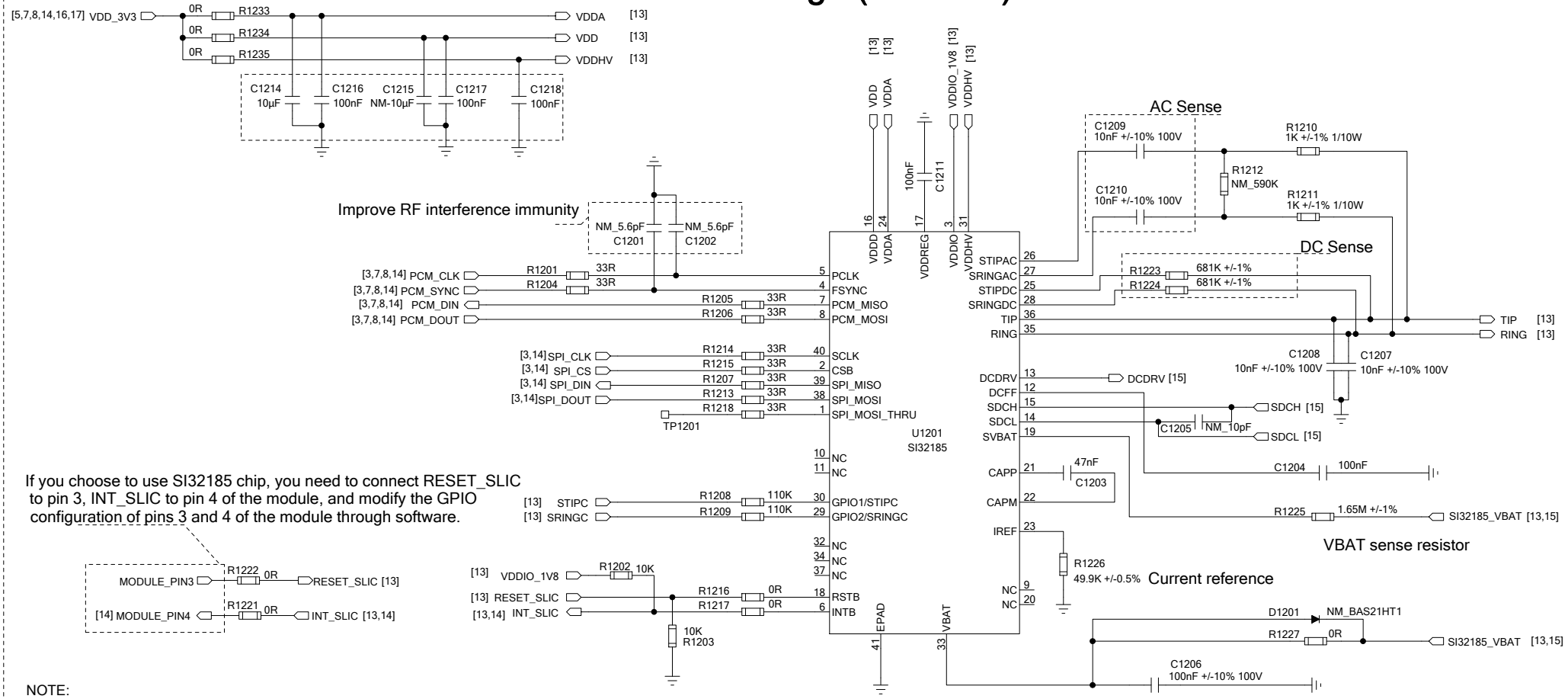
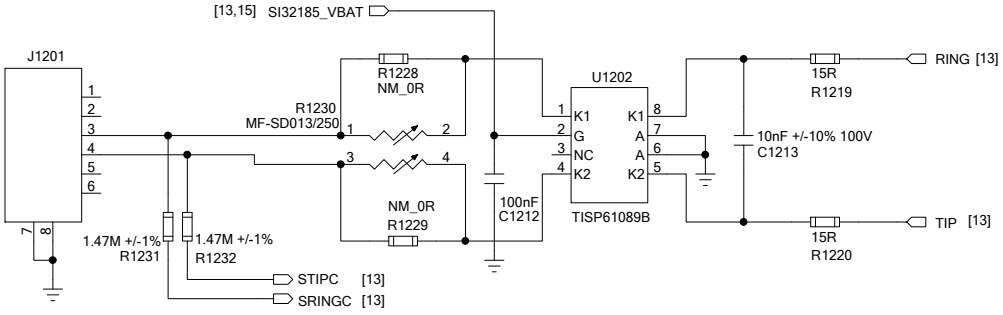
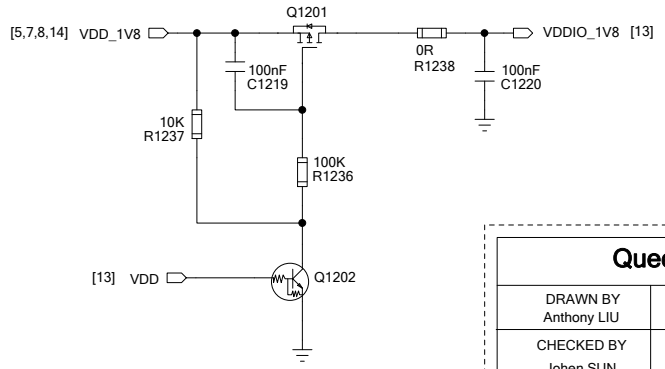
SLIC Design (SI32185)



NOTE:
For more details, please refer to the datasheet of SI32185.

High Voltage Ringing SLIC Protector





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CHECKED BY Johen SUN	SIZE A2	VER 1.0
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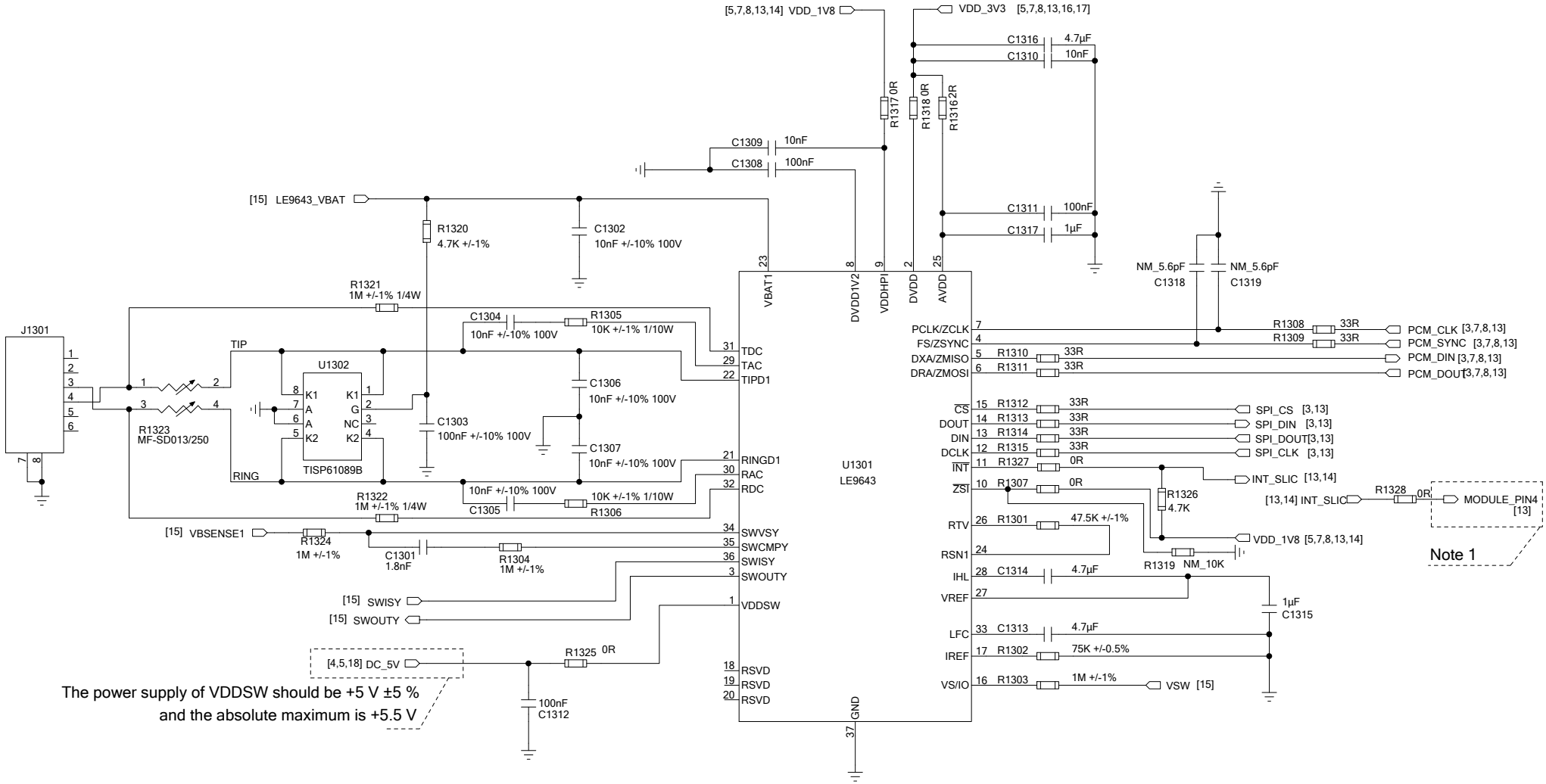
SLIC Design (LE9643)



NOTE:

1. If you need int function, you need to connect INT_SLIC to pin 4 of the module, and modify the GPIO configuration of pin 4 of the module through software.
2. For more details, please refer to the datasheet of LE9643.

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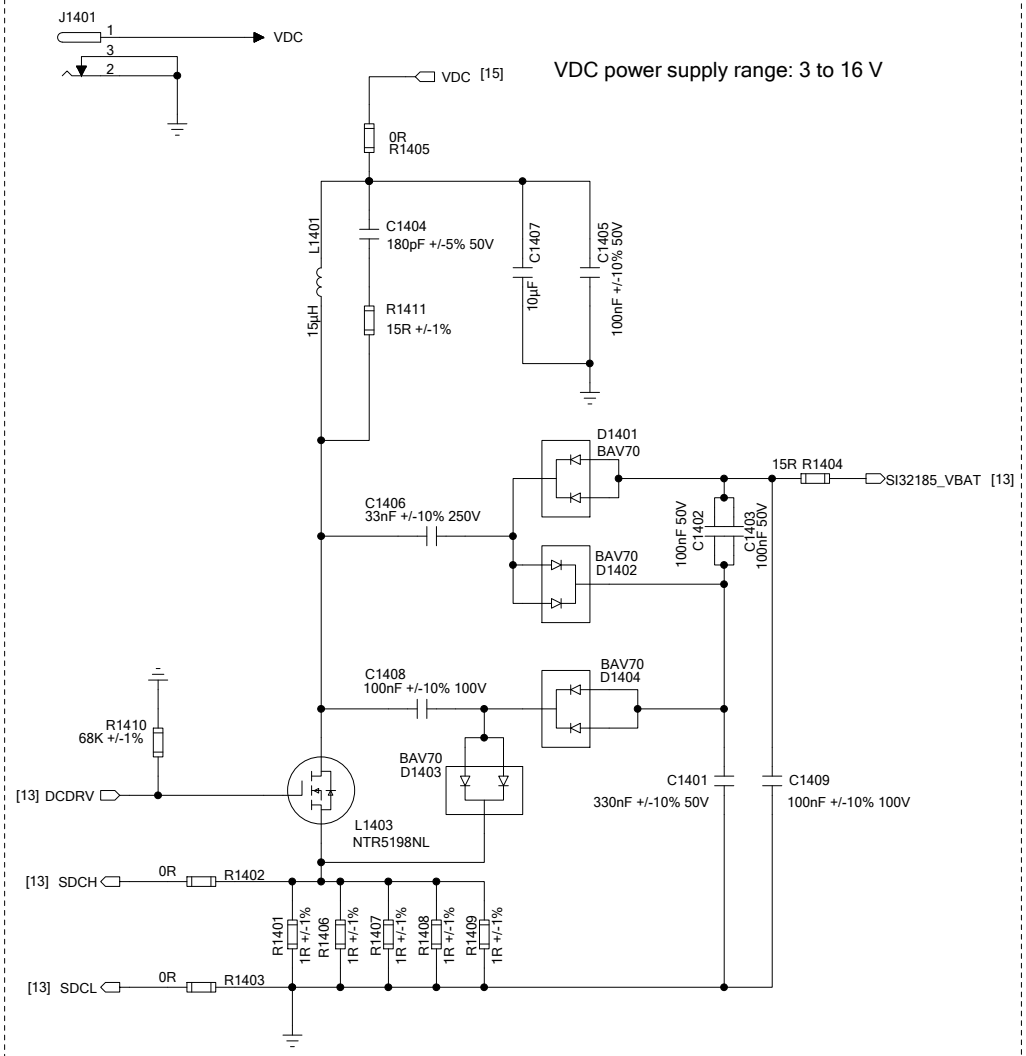
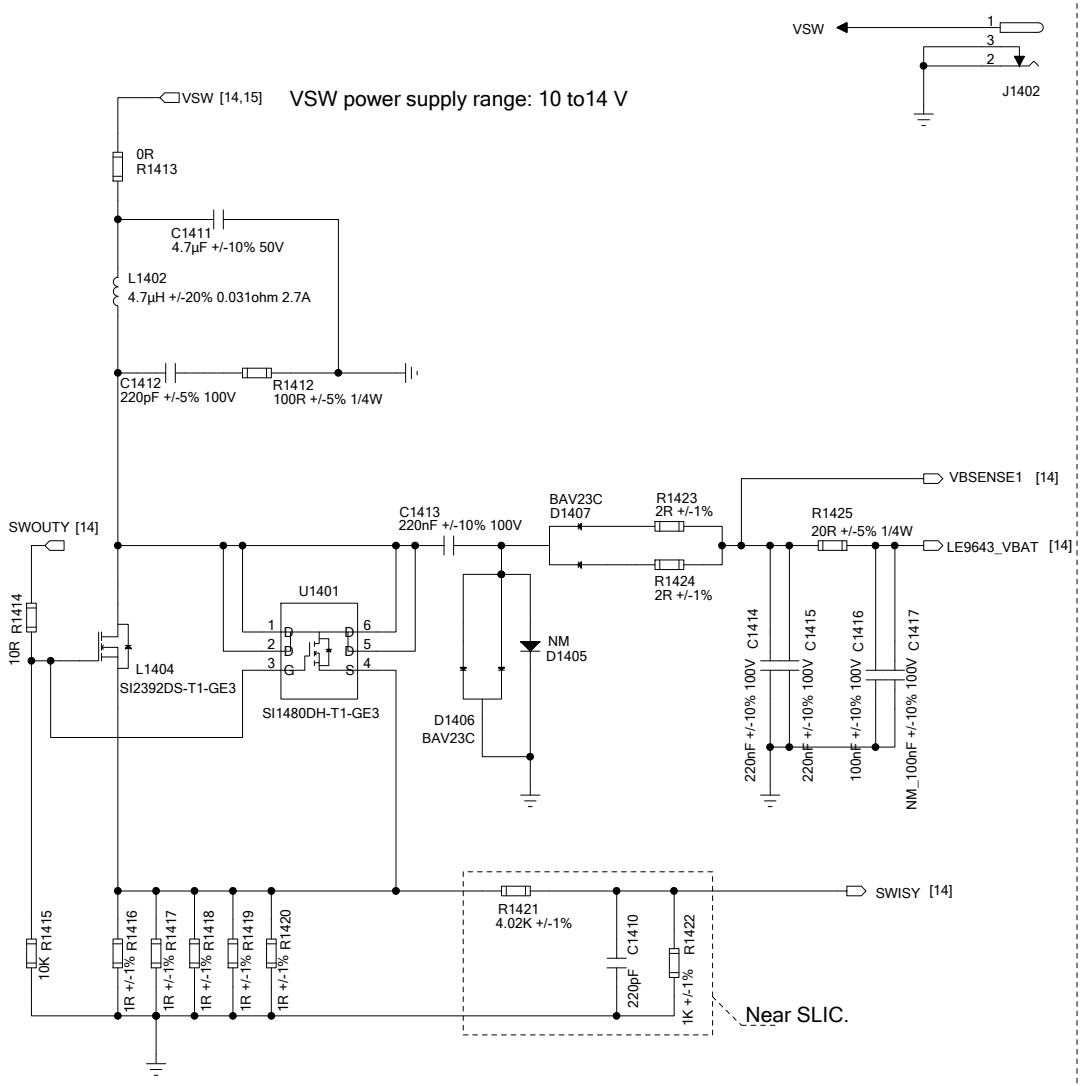
SLIC Power Supply Design

SI32185 Power Supply Design



LE9643 Power Supply Design



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CHECKED BY Johen SUN	SIZE A2	VER 1.0
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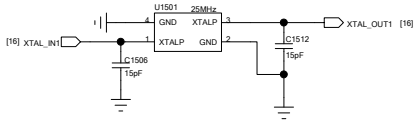
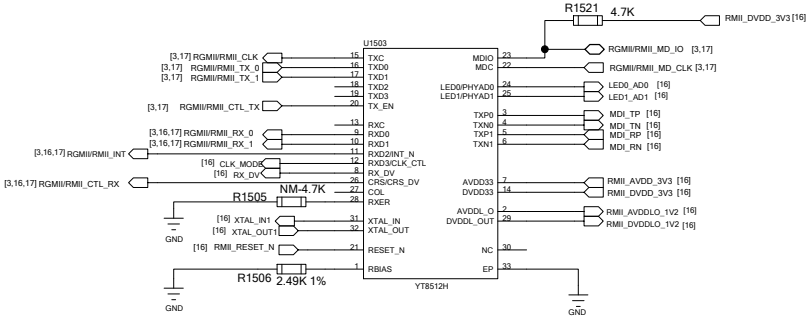
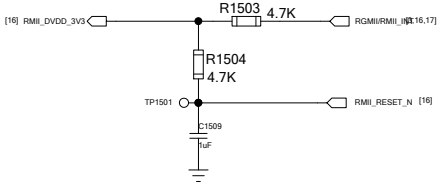
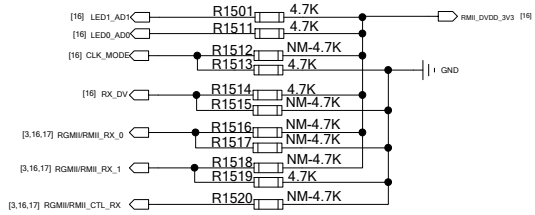
RMII Design (100 Mbps Ethernet)

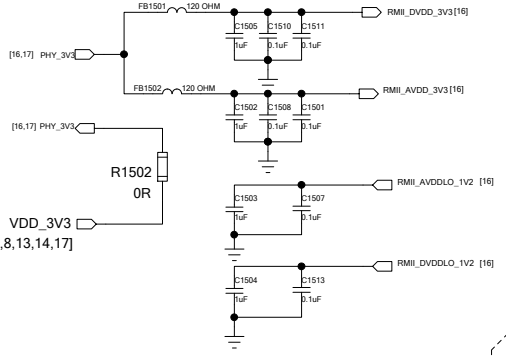


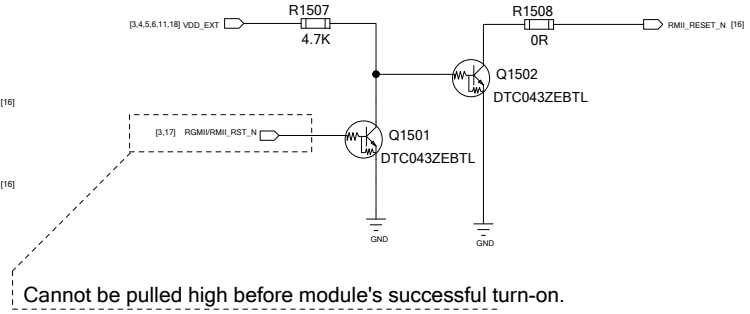




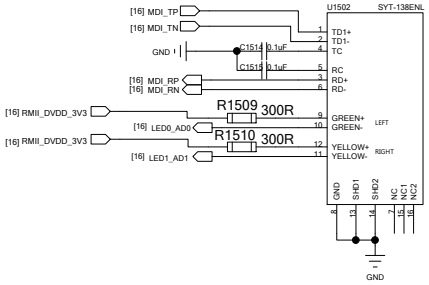
Option Setting







Cannot be pulled high before module's successful turn-on.



NOTE:

1. Keep RMII and RGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
2. The single-ended impedance of RGMII data trace is 50 Ω ±10 %.
3. The length difference of RGMII/RMII_TX_[0:1], RGMII_TX_[2:3], RGMII/RMII_CTL_TX, RGMII_CK_TX should be less than 2 mm, and the spaceing between the signal traces should be larger than 2 times of trace width. Similarly, the length difference of RGMII/RMII_RX_[0:1], RGMII_RX_[2:3], RGMII/RMII_CTL_RX, RGMII/RMII_CLK should be less than 2 mm, and the spaceing between the signal traces should be larger than 2 times of trace width.
4. Spacing between Tx bus and Rx bus is larger than 2.5 times of the trace width.
5. Spacing between Tx bus or Rx bus is larger than 3 times of the trace width.
6. It is recommended to use a level conversion chip without pull-up for the level-shifting circuit.
7. For more details, please refer to the datasheet of YT8512H.

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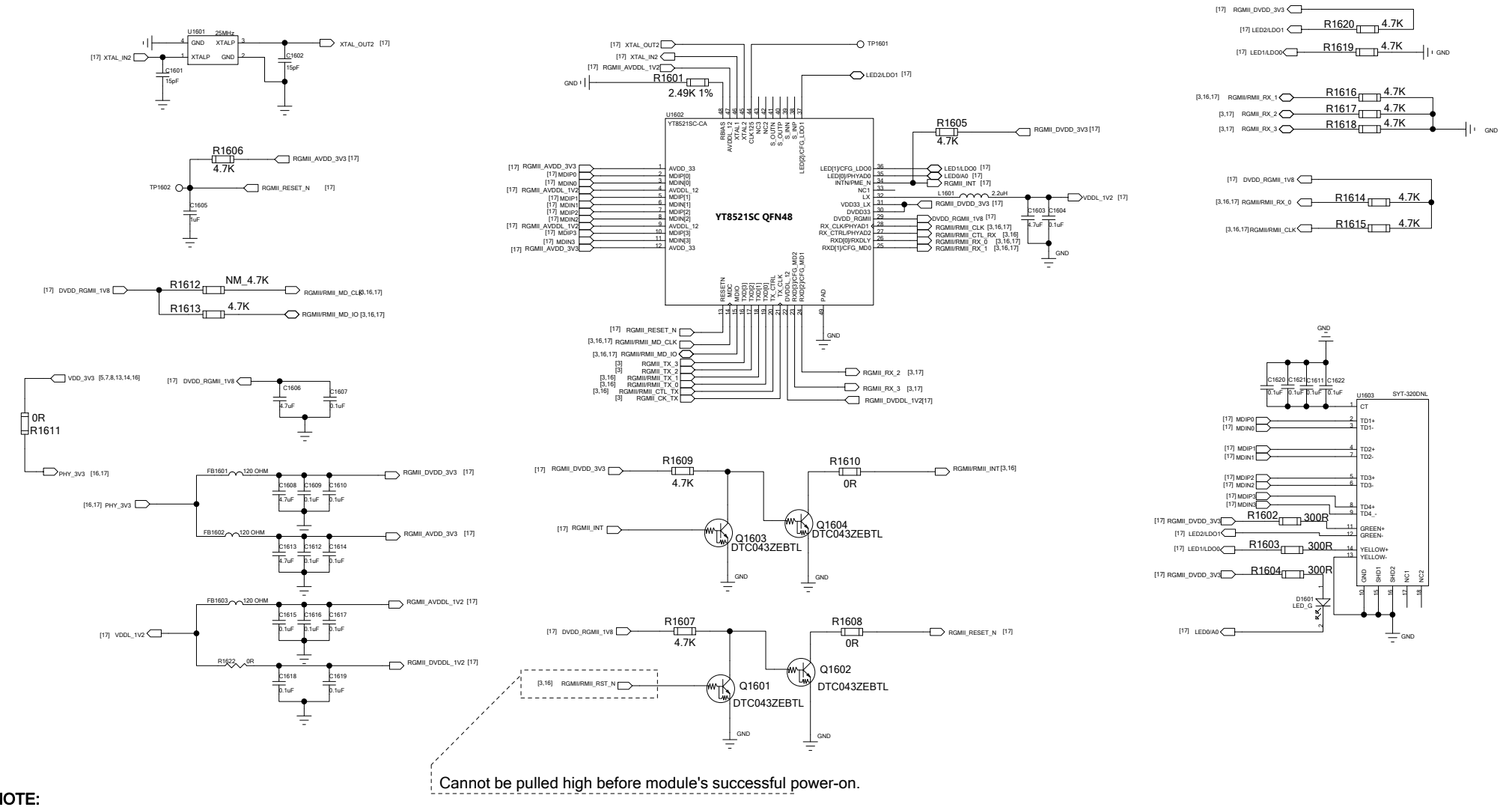
RGMII Design (1000 Mbps Ethernet)



NOTE:

1. Keep RMII and RGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
2. The single-ended impedance of RGMII data trace is 50 Ω ±10 %.
3. The length difference of RGMII/RMII_TX_[0:1], RGMII_TX_[2:3], RGMII/RMII_CTL_TX, RGMII_CK_TX should be less than 2 mm, and the space between the signal traces should be larger than 2 times of trace width. Similarly, the length difference of RGMII/RMII_RX_[0:1], RGMII_RX_[2:3], RGMII/RMII_CTL_RX, RGMII/RMII_CLK should be less than 2 mm, and the space between the signal traces should be larger than 2 times of trace width.
4. Spacing between Tx bus and Rx bus is larger than 2.5 times of the trace width.
5. Spacing between Tx bus or Rx bus is larger than 3 times of the trace width.
6. It is recommended to use a level conversion chip without pull-up for the level-shifting circuit.
7. For more details, please refer to the datasheet of YT8521S.

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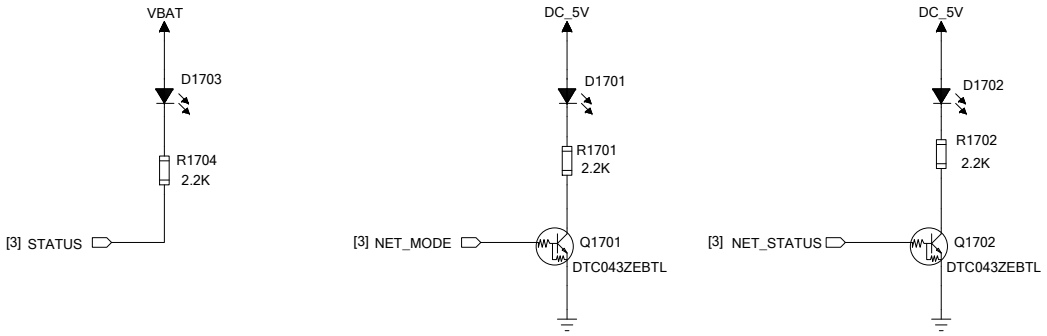
Other Designs

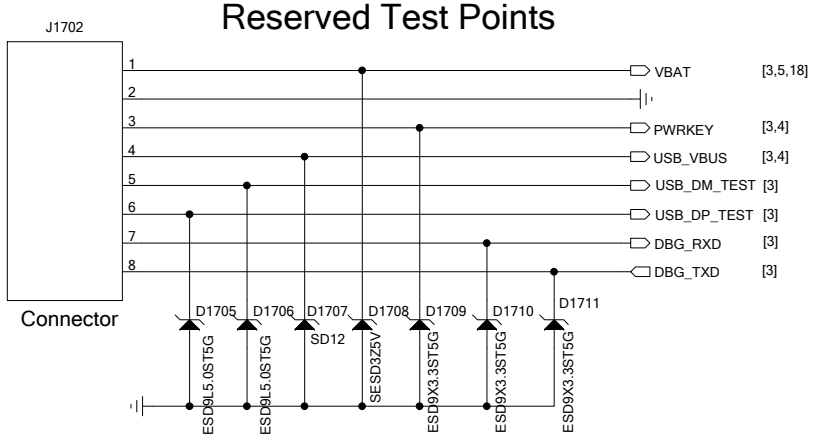
Indicators



NOTE:

1. The STATUS is an open drain output pin.
2. For more details about NET_MODE and NET_STATUS, please refer to *Quectel_EC200A_Series_Hardware_Design*.
3. If the low current consumption is required when the your device is in sleep, replace the power supply VBAT of STATUS, DC_5V of NET_MODE and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

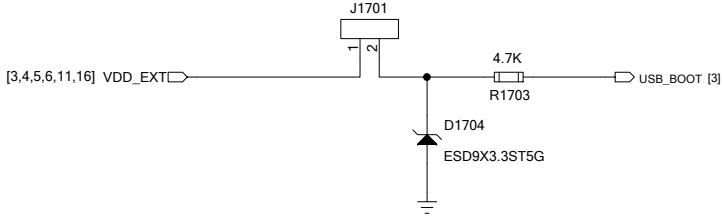
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for catching logs.
2. Test points for USB interface also can be reserved for firmware upgrade.
3. The junction capacitance of the ESD protection componets on USB data traces should be less than 2 pF.
4. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V.

Emergency Download



NOTE:

1. It is recommended to reserve the USB_BOOT interface design.
2. USB_BOOT is kept open by default.
   Pull up USB_BOOT to VDD_EXT to make the module enter emergency download mode before it is turned on.

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