M65 QuecOpen

Hardware Design

GSM/GPRS Module Series

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The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating M65 QuecOpen module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

About the Document

Revision History

Version	Date	Author	Description
-	2019-08-31	Claude WEI	Creation of the document
1.0	2021-06-24	Claude WEI/ Zeki XU	First official release

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1 Introduction

This document defines the M65 QuecOpen module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand M65 QuecOpen module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, customers can use M65 QuecOpen to design and set mobile applications easily.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Concept

2.1. General Description

QuecOpen® is a solution that uses the module as the main processor. With the development of communication technology and changes in market demand, more and more customers have realized the advantages of QuecOpen solutions. In particular, its advantages in reducing product costs have made it popular among industry users. Using the QuecOpen solution can simplify the user's development process for wireless applications and simplify the hardware structure design, thereby reducing product costs. The main features of the QuecOpen solution are as follows:

- Quickly develop embedded applications and shorten product development cycle
- No external processor, memory and discrete and related design costs
- Reduce the actual size of the end product
- Reduce product power consumption
- Upgrade firmware remotely through QuecOpen DFOTA
- Enhance product safety through anti-copy technology
- Improve the market price performance and competitiveness

M65 QuecOpen is an industrial grade quad-band GSM/GPRS module with working frequencies of GSM850 MHz, EGSM900 MHz, DCS1800 MHz and PCS1900 MHz. Providing GPRS data transmission and GSM SMS service, M65 QuecOpen supports GPRS multi-slot class 1–12 (Class 12 by default) and GPRS coding schemes CS-1, CS-2, CS-3 and CS-4.

M65 QuecOpen is an SMD type module with LCC package, which can be easily embedded into applications. It provides abundant hardware interfaces.

With the ultra-small size of 17.7 mm ×15.8 mm × 2.4 mm, M65 QuecOpen can meet almost all the requirements for M2M applications, including vehicles, personal tracking, security system, wireless POS, industrial PDA, smart metering, remote maintenance and control, etc.

Designed with power saving technique, the current consumption of M65 QuecOpen is as low as 1.2 mA in sleep mode when DRX is 5.

M65 QuecOpen integrates various Internet service protocols, such as TCP, UDP, FTP and PPP. Extended AT commands have been developed so that users can use these Internet service protocols easily.

M65 QuecOpen module is fully compliant with EU RoHS directive.

2.2. Key Features

The following table describes the features of M65 QuecOpen module.

Table 2: Key Features

Features	Description
Power Supply	● Single supply voltage: 3.45–4.25 V ● Typical supply voltage: 4.0 V
Power Saving	Typical power consumption in sleep mode: ● 1.2 mA @ DRX = 5 ● 1.1 mA @ DRX = 9
Frequency Bands	● Quad-band: GSM850, EGSM900, DCS1800, PCS1900 ● The frequency bands can be searched automatically ● The frequency bands can be set by AT commands ● Compliant to GSM Phase 2/2+
GSM Power Class	● Class 4 (2 W) at GSM850 and EGSM900 ● Class 1 (1 W) at DCS1800 and PCS1900
GPRS Connectivity	● GPRS multi-slot class 12 (default) ● GPRS multi-slot class 1–12 (configurable) ● GPRS mobile station class B
GPRS Data Features	● GPRS data downlink transmission rate: max. 85.6 kbps ● GPRS data uplink transmission rate: max. 85.6 kbps ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Support PAP and CHAP protocols which are usually used for PPP connection ● Support Internet service protocols: TCP/UDP/PPP/HTTP/NTP/PING/ IPv6/TTS/FTP/SSL/MQTT ● Support USSD (Unstructured Supplementary Service Data)
Temperature Ranges	● Operating temperature range: -35 °C to +75 °C [1)] ● Extended temperature range: -40 °C to +85 °C [2)] ● Storage temperature range: -40 °C to +90 °C
SMS	● Text and PDU mode ● SMS storage: (U)SIM card
(U)SIM Interface	Support (U)SIM card: 1.8 V and 3.0 V
Audio Features	Speech codec modes: ● Half rate (ETS 06.20) ● Full rate (ETS 06.10)

	● Enhanced full rate (ETS 06.50/06.60/06.80) ● Adaptive multi-rate (AMR) ● Echo suppression ● Noise reduction
UART Interfaces	**Main UART port:** ● Full-function UART port ● Used for AT command communication and GPRS data transmission ● Support adaptive baud rate from 4800 bps to 115200 bps **Debug UART port:** ● Used for firmware upgrading and debugging ● Fixed baud rates: 921600 bps **Auxiliary UART port:** ● Used for AT command communication only
Phonebook Management	Support phonebook types: SM, ME, ON, MC, RC, DC, LD, LA
(U)SIM Application Toolkit	Support SAT Class 3, GSM 11.14 Release 99
Real Time Clock (RTC)	Supported
Physical Characteristics	● Size: (17.7 ±0.15) mm × (15.8 ±0.15) mm × (2.4 ±0.2) mm ● Package: LCC ● Weight: Approx. 1.1 g
Firmware Upgrade	● Firmware upgrade via debug UART port or DFOTA
Antenna Interface	● GSM antenna interface ● 50 Ω impedance

NOTE

1. [1)] Within the operation temperature range, the module is 3GPP compliant.
2. [2)] Within the extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on the radio spectrum and no harm to the radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.

Table 3: Coding Schemes and Maximum Net Data Rates over Air Interface

Coding Scheme	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	9.05 kbps	18.1 kbps	36.2 kbps
CS-2	13.4 kbps	26.8 kbps	53.6 kbps

CS-3	15.6 kbps	31.2 kbps	62.4 kbps
CS-4	21.4 kbps	42.8 kbps	85.6 kbps

2.3. Functional Diagram

The following figure shows a block diagram of M65 QuecOpen and illustrates the major functional parts.

- Power Management
- Memory
- Radio Frequency
- Peripheral Interfaces
  - — Power Supply
  - — PWRKEY
  - — UART Interfaces
  - — Audio Interfaces
  - — PCM Interface*
  - — (U)SIM Interface
  - — ADC Interface
  - — RF Interface
  - — GPIO Interfaces

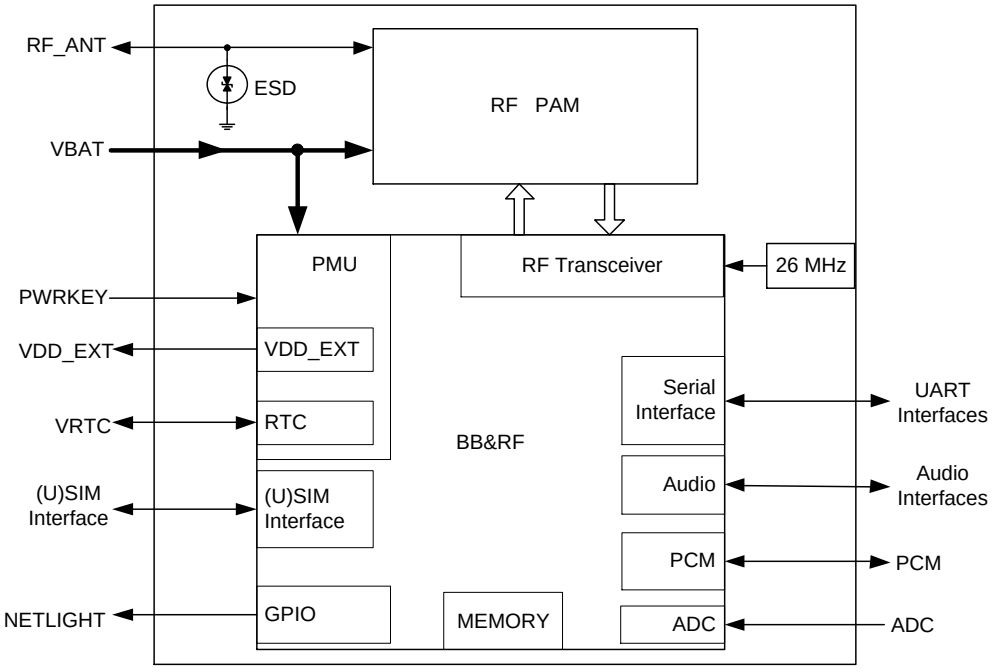

Figure 1: Module Functional Diagram

2.4. Evaluation Board

Quectel provides a complete set of development tools to facilitate the use and testing of M65 QuecOpen module. The development tools include a GSM-EVB (evaluation board), USB to RS-232 cable, micro USB cable, power adapter, antenna, RF components, etc. For details, refer to ***document [3]***.

3 Application Interfaces

3.1. General Description

The module adopting LCC package has 44 pins. The subsequent chapters will provide detailed descriptions of the following interfaces/functions:

- Power supply
- Power-on/off scenarios
- Power saving
- RTC backup power
- UART interfaces
- Audio interfaces
- I2C interface
- (U)SIM interface
- ADC interface
- RI behaviors
- Network status indication
- RF transmitting signal indication
- GPIO interfaces
- External interrupt

3.2. Pin Assignment

The following figure shows the pin assignment of M65 QuecOpen.

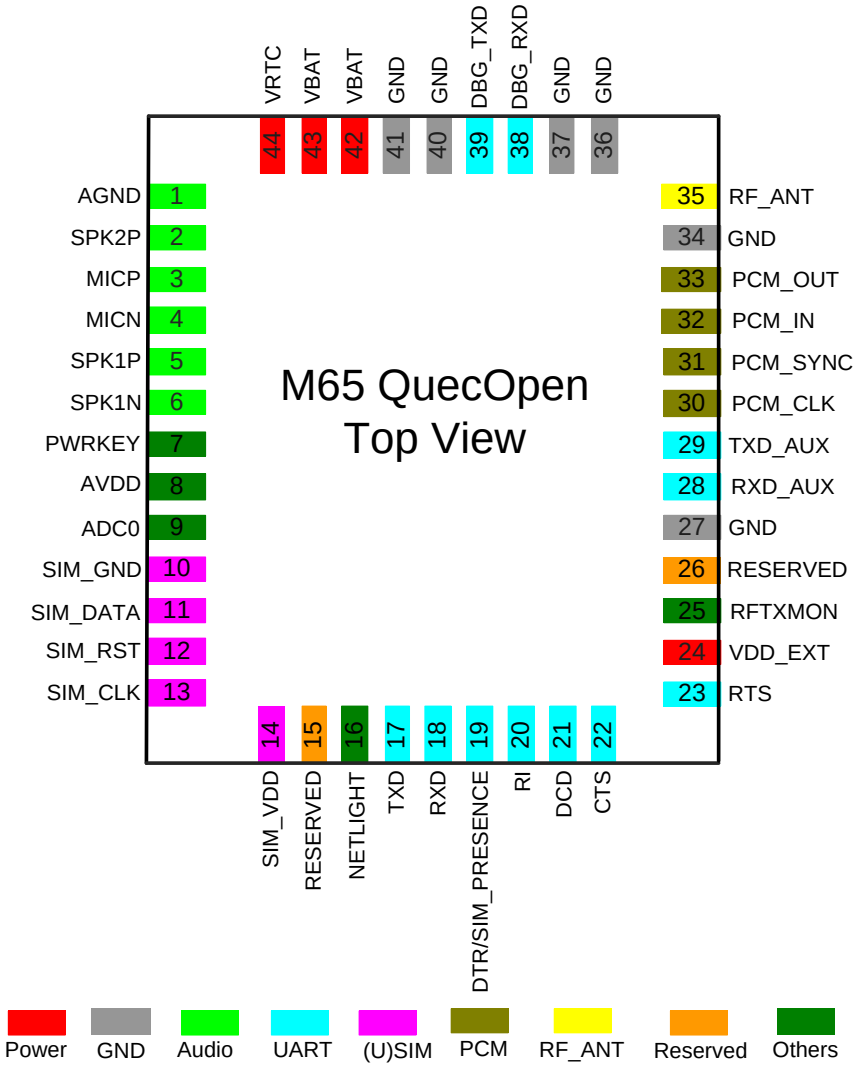

Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED or unused pins unconnected.
2. All GND pins should be connected to ground.

3.3. Pin Description

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output
PIO	Power Input/Output

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Main power supply of the module	$V_I$max = 4.25 V $V_I$min = 3.45 V $V_I$nom = 4.0 V	It must be provided with sufficient current up to 2.0 A.
VRTC	44	PIO	Input: Supply power to RTC when VBAT is removed Output: Charge for backup battery or ultra-capacitor when VBAT is applied	$V_I$max = 3.5 V $V_I$min = 3.0 V $V_I$nom = 3.3 V $V_O$max = 3.39 V $V_O$min = 2.99 V $V_O$nom = 3.1 V $I_O$max = 1.9 mA Iin≈21 μA	If unused, keep this pin unconnected.
VDD_EXT	24	PO	Supply 2.8 V voltage for external circuit	$V_O$max = 2.9 V $V_O$min = 2.7 V $V_O$nom = 2.8 V $I_O$max = 20 mA	1. If unused, keep this pin unconnected. 2. It is

					recommended to add a 2.2–4.7 μF bypass capacitor when using this pin to supply power to external circuits.
GND	27, 34 36, 37 40, 41		Ground		
PWRKEY					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	V_{IL}max = 0.1 × VBAT V_{IH}min = 0.6 × VBAT V_{IH}max = 3.1 V	
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MICP, MICN	3, 4	AI	Audio differential input channel	Refer to ***Chapter 3.12***	If unused, keep these pins unconnected.
SPK1P, SPK1N	5, 6	AO	Audio differential output channel 1		If unused, keep these pins unconnected.
SPK2P	2	AO	Audio single-ended output channel 2		If unused, keep this pin unconnected.
AGND	1		Analog ground. Separate ground connection for external audio circuits.		
Network Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NETLIGHT	16	DO	Network status indication	V_{OH}min = 0.85 × VDD_EXT V_{OL}max =	If unused, keep this pin unconnected.

				0.15 × VDD_EXT	
Main UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TXD	17	DO	Transmit data	V_{IL}min = 0 V V_{IL}max = 0.25 × VDD_EXT V_{IH}min = 0.75 × VDD_EXT V_{IH}max = VDD_EXT + 0.2 V_{OH}min = 0.85 × VDD_EXT V_{OL}max = 0.15 × VDD_EXT	If only TXD, RXD and GND are used for communication, it is recommended to keep all the other pins unconnected.
RXD	18	DI	Receive data		
DTR	19	DI	Data terminal ready		
RI	20	DO	Ring indication		
DCD	21	DO	Data carrier detection		
CTS	22	DO	Clear to send		
RTS	23	DI	Request to send		
Debug UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	39	DO	Debug UART transmit	V_{IL}min = 0 V V_{IL}max = 0.25 × VDD_EXT	If unused, keep this pin unconnected.
DBG_RXD	38	DI	Debug UART receive	V_{IH}min = 0.75 × VDD_EXT V_{IH}max = VDD_EXT + 0.2 V_{OH}min = 0.85 × VDD_EXT V_{OL}max = 0.15 × VDD_EXT	If unused, keep this pin unconnected.
Auxiliary UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TXD_AUX	29	DO	Transmit data	V_{IL}min = 0 V V_{IL}max = 0.25 × VDD_EXT	If unused, keep this pin unconnected.
RXD_AUX	28	DI	Receive data	V_{IH}min = 0.75 × VDD_EXT V_{IH}max = VDD_EXT + 0.2 V_{OH}min = 0.85 × VDD_EXT	If unused, keep this pin unconnected.

				V_{OL}max = 0.15 × VDD_EXT	
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SIM_VDD	14	PO	Power supply for (U)SIM card	Either 1.8 V or 3.0 V, selected by software automatically.	All signals of (U)SIM interface should be protected against ESD with a TVS diode array. The maximum trace length from the module pad to (U)SIM card connector is 200 mm.
SIM_CLK	13	DO	(U)SIM card clock	V_{OL}max = 0.15 × SIM_VDD V_{OH}min = 0.85 × SIM_VDD	
SIM_DATA	11	DIO	(U)SIM card data	V_{IL}max = 0.25 × SIM_VDD V_{IH}min = 0.75 × SIM_VDD V_{OL}max = 0.15 × SIM_VDD V_{OH}min = 0.85 × SIM_VDD	
SIM_RST	12	DO	(U)SIM card reset	V_{OL}max = 0.15 × SIM_VDD V_{OH}min = 0.85 × SIM_VDD	
SIM_GND	10		Ground specified for (U)SIM card		
SIM_ PRESENCE	19	DI	(U)SIM card insertion detection	V_{IL}min = 0V V_{IL}max = 0.25 × VDD_EXT V_{IH}min = 0.75 × VDD_EXT V_{IH}max = VDD_EXT + 0.2	Multiplexing function as DTR by default.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AVDD	8	PO	Reference voltage of ADC circuit	$V_O$max = 2.9 V $V_O$min = 2.7 V $V_O$nom = 2.8 V	If unused, keep this pin unconnected.
ADC0	9	AI	General-purpose ADC Interface	Voltage range: 0–1.8 V	If unused, keep this pin unconnected.
PCM Interfaces*					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCM_ CLK	30	DO	PCM clock	V_{IL}min = 0 V V_{IL}max = 0.25 × VDD_EXT V_{IH}min = 0.75 × VDD_EXT V_{IH}max = VDD_EXT + 0.2 V_{OH}min = 0.85 × VDD_EXT V_{OL}max = 0.15 × VDD_EXT	If unused, keep this pin unconnected.
PCM_ SYNC	31	DO	PCM data frame synchronization		If unused, keep this pin unconnected.
PCM_IN	32	DI	PCM data input		If unused, keep this pin unconnected.
PCM_OUT	33	DO	PCM data output		If unused, keep this pin unconnected.
Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RF_ANT	35	AIO	GSM antenna interface		50 Ω impedance
Transmitting Signal Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RFTXMON	25	DO	RF transmitting signal indication	V_{OH}min = 0.85 × VDD_EXT V_{OL}max = 0.15 × VDD_EXT	If unused, keep this pin unconnected.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	15, 26				Keep these pins unconnected.
GPIO		DIO		V_{OL}max = VDD_EXT V_{OH}min = 2.0 V V_{IL}max = 0.67 V V_{IH}min =1.7 V V_{IH}max = VDD_EXT + 0.3 V	If unused, keep this pin unconnected.

Table 6: Multiplexing function

Pin Name	Pin No.	Mode 1 (Default)	Mode 2	Mode 3	Mode 4
NETLIGHT	16	NETLIGHT	GPIO	EINT	*
DTR	19	DTR	GPIO	EINT	*
RI	20	RI	GPIO	I2C2_SCL	EINT
DCD	21	DCD	GPIO	I2C2_SDA	EINT
CTS	22	CTS	GPIO	EINT	*
RTS	23	RTS	GPIO	EINT	*
RFTXMON	25	RFTXMON	GPIO	EINT	*
RXD_AUX	28	RXD_AUX	GPIO	EINT	*
TXD_AUX	29	TXD_AUX	GPIO	EINT	*
PCM_CLK	30	PCM_CLK	GPIO	EINT	*
PCM_SYNC	31	PCM_SYNC	GPIO	EINT	*
PCM_IN	32	PCM_IN	GPIO	EINT	*
PCM_OUT	33	PCM_OUT	GPIO	EINT	*

3.4. Operating Modes

The following table briefly describes the various working modes of M65 QuecOpen module.

Table 7: Overview of Operating Modes

Mode	Details	
Normal operation	GSM/GPRS sleep	After enabling sleep mode by **AT+QSCLK=1**, the module will automatically enter sleep mode if DTR is set to high level and there is no interrupt (such as GPIO interrupt or data on UART interface). In this case, the current consumption of module will reduce to the minimal level. During sleep mode, the module can still receive paging message and SMS from the system normally.

	GSM idle	The software is active. The module has registered on the GSM network and is ready to send and receive GSM data.
	GSM talk	The module is connected to network, its power consumption is decided by the configuration of power control level (PCL), dynamic DTX control and the working RF band.
	GPRS idle	The module is not registered on GPRS network nor reachable through GPRS channel.
	GPRS standby	The module is registered on GPRS network without active GPRS PDP context. The SGSN knows the routing area where the module is located at.
	GPRS ready	The PDP context is active without data transfer. The module is ready to receive or send GPRS data. The SGSN knows the cell where the module is located at.
	GPRS data	There is GPRS data in transfer. In this mode, the power consumption of module is decided by the PCL, working RF band and GPRS multi-slot configuration.
Power down mode	The normal shutdown can be realized by sending **AT+QPOWD=1**, *Ql_PowerDown()* function or using PWRKEY under the condition of keeping VBAT powered on. In this case, operating voltage (connected to VBAT) remains applied; the power management ASIC disconnects the power supply from the baseband part of the module while only power supply for RTC is remained. The software is not active and the UART interface is not accessible.	
Minimum functionality mode (without removing power supply)	**AT+CFUN=0** can be used to set the module to minimum functionality mode without removing the power supply. In this case, either RF function or (U)SIM card is invalid; but the UART interface is still accessible. In this case, the power consumption is very low.	

3.5. Flash Memory Capacity Allocation

The module is embedded with a 32 Mbit flash memory, and the memory capacity is allocated as follows:

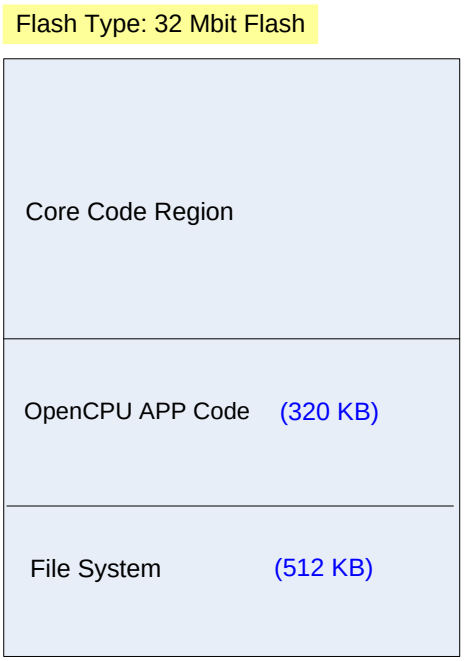

Figure 3: Flash Memory Capacity Allocation

M65 QuecOpen allocates 320 KB of storage space to programme code , and 512 KB of file system space to store data related to file operations, such as system configuration files, temporary data, images, and multimedia files.

- RAM (Random Access Memory)

M65 QuecOpen provides 100 KB of RAM space for embedded applications, also provides 500 KB of dynamic memory.

3.6. Power Supply

3.6.1. Power Features

Power supply design is an important part of M65 QuecOpen application design. Due to the 577 μs burst in GSM part every 4.615 ms. In a burst period, power supply should deliver high peak current and the supply voltage should not drop below the minimum working voltage.

The maximum current consumption of the module could reach 2.0 A during a burst transmission, which will cause a large voltage drop on VBAT. In order to ensure the stability of the module's operation, it is recommended that the maximum voltage drop during the burst transmission should not exceed 400 mV.

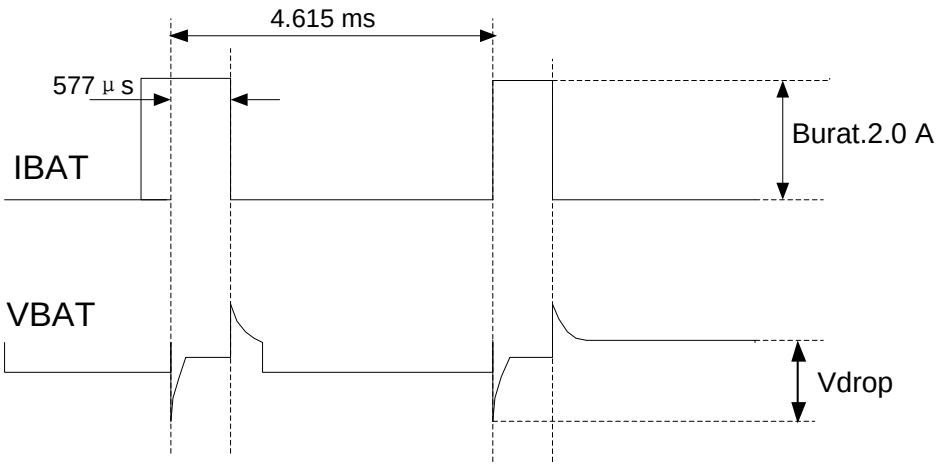

Figure 4: Voltage Ripple during Transmission

3.6.2. Decrease Supply Voltage Drop

The power supply range of the module is from 3.45 V to 4.25 V. Make sure that the input voltage will never drop below 3.45 V even in a burst transmission. If the power voltage drops below 3.45 V, the module could be turned off automatically. For better power performance, it is recommended to place a 100 µF tantalum capacitor with low ESR (ESR = 0.7 Ω), ceramic capacitors of 100 nF, 33 pF and 10 pF, and TVS near the VBAT pin. The reference circuit is illustrated in the following figure.

The VBAT trace should be wide enough to ensure that there is not too much voltage drop during burst transmission. The width of VBAT trace should be no less than 2 mm; and in principle, the longer the trace is, the wider it will be.

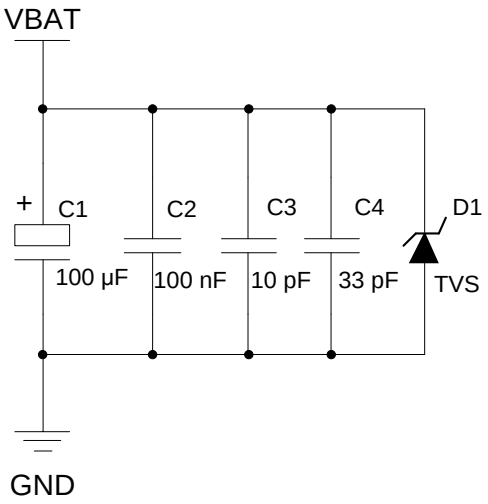

Figure 5: Reference Circuit for VBAT Input

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be provided with sufficient current up to 2.0 A. If the voltage difference between the input and output is not too big, it is suggested to use an LDO to supply power for the module; if there is a big voltage difference, a switcher power converter is preferred to be used.

The following figure shows a reference design for +5 V input power supply. The designed output voltage for the power supply is 4.0 V and the maximum load current is 3.0 A. In order to ensure the stability of the output voltage, a zener diode is suggested to be placed close to VBAT pin. To ensure the stability of the output power supply, it is recommended to reserve a TVS tube at the output end and place it close to the VBAT pin of the module.

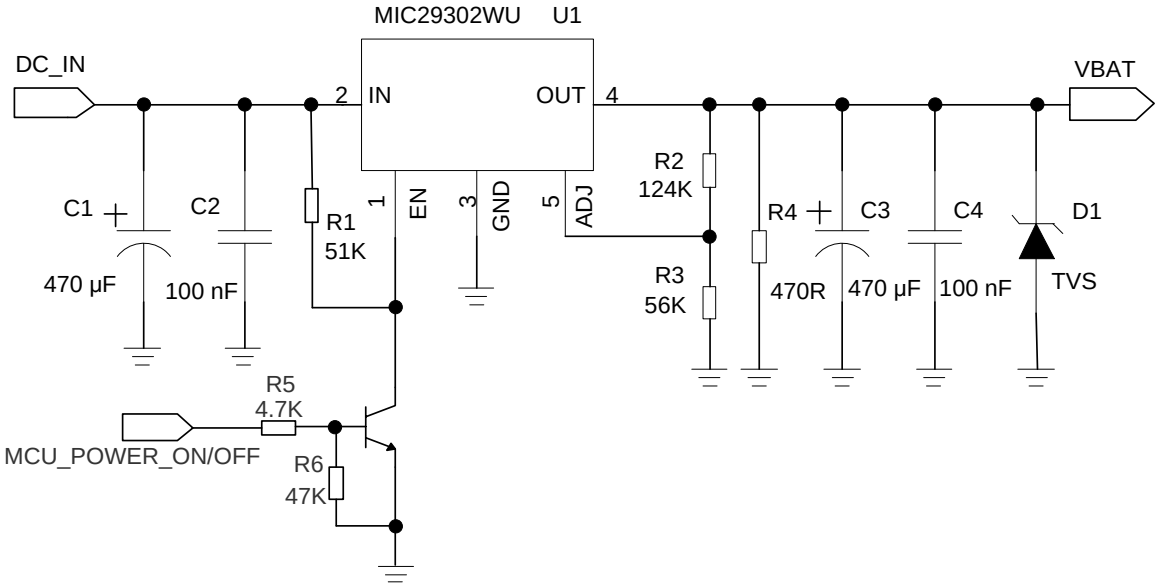

Figure 6: Reference Design for Power Supply

NOTE

It is suggested to control the module's main power supply (VBAT) via LDO enable pin to restart the module when the module becomes abnormal. Power switch circuit like P-channel MOSFET switch circuit can also be used to control VBAT.

3.6.4. Monitor Power Supply

AT+CBC can be used to monitor the supply voltage of the module. The unit is mV. For details, refer to the ***document [1]***.

3.7. Power-on/off Scenarios

3.7.1. Power-on

M65 QuecOpen module can be turned on by driving PWRKEY to a low level for 1.2 s. It is recommended use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated as below.

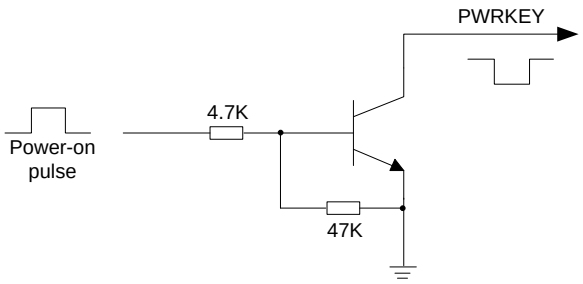

Figure 7: Power on Module through an Open Collector Driver

NOTE

1. M65 QuecOpen is set to adaptive baud rate mode (**AT+IPR=0**) by default; in this mode, after the module is powered on, URC "RDY" is not reported to the host controller. AT commands can be received by the module in 4–5 s after it is powered on. Host controller should first send an "**AT**" to the module so that the module can detect host controller's baud rate, and then continue to send the next "**AT**" until "**OK**" is received. Then **AT+IPR=x;&W** should be sent to set a fixed baud rate for the module and save the configuration to its flash memory. After the configuration is completed, URC "RDY" would be received from the main UART interface when the module is powered on. For more details, refer to the related content of **AT+IPR** in ***document [1]***.
2. If the AT command is responded, it indicates the module is turned on successfully; otherwise, it indicates the module fails to be turned on.

The other way to control the PWRKEY is using a button directly. While pressing the button, an electrostatic strike may generate from the finger, and thus, a TVS is indispensable to be placed nearby the button for ESD protection and also for the best performance. A reference circuit is shown in the following figure.

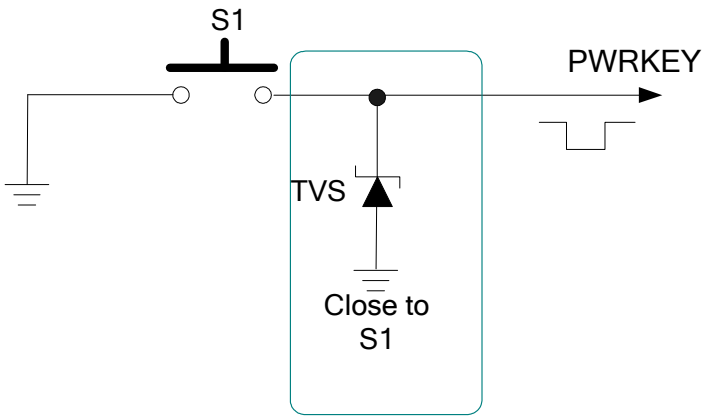

Figure 8: Power on the Module through a Button

The power-on scenario is illustrated in the following figure.

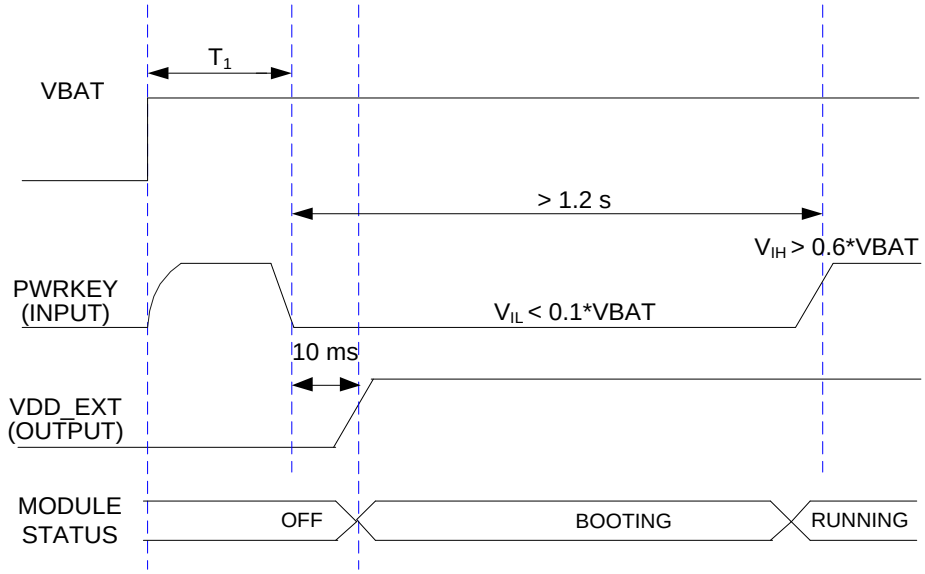

Figure 9: Timing of Powering on the Module

NOTE

Ensure that the VBAT voltage is stable before pulling down the PWRKEY and keep the interval no less than 100 ms.

3.7.2. Power-off

Either of the following procedures can be used to turn off the module:

- Normal power-off procedure: Turn off the module using PWRKEY.
- Normal power-off procedure: Turn off the module using **AT+QPOWD=1**.
- Under-voltage automatic shutdown: Take effect when under-voltage is detected.

3.7.2.1. Turn off the Module Using PWRKEY

It is a safe way to turn off the module by driving PWRKEY low for a certain time (1–1.2 s). The timing of turning off the module is illustrated below.

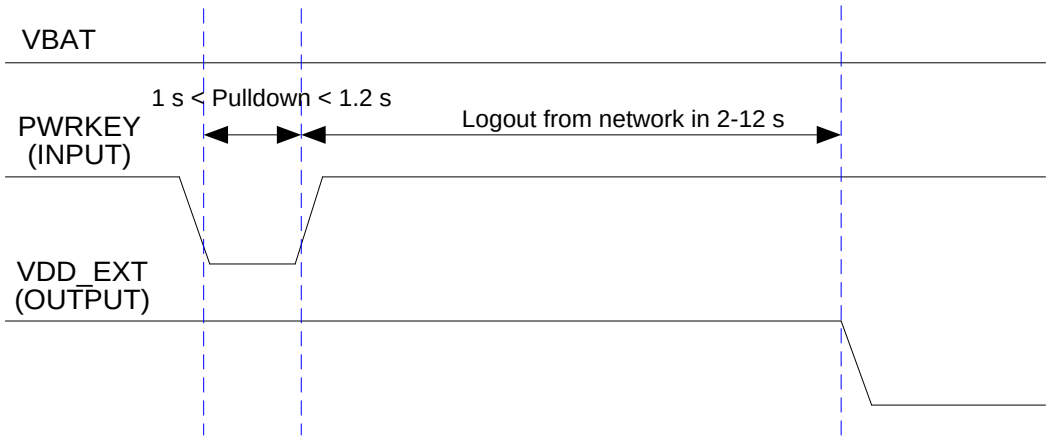

Figure 10: Timing of Turning off the Module

The power-off procedure causes the module to log off from the network and allows the firmware to save important data before completely disconnecting from the power supply.

Before the completion of the power-off procedure, the module sends out the URC shown below:

NORMAL POWER DOWN

Since then, no further AT commands can be executed. Then the module enters power-down mode, while RTC is still active.

NOTE

1. The URC does not appear when adaptive baud rate is applied and DTE and DCE are not correctly synchronized after start-up. It is recommended to set the module to a fixed baud rate.
2. Since the time to log off the network is related to the local mobile network, it is recommended to disconnect the power supply or restart the module after a delay of about 12 seconds.

3.7.2.2. Turn off the Module Using AT Command

It is also a safe way to turn off the module via **AT+QPOWD=1**, which can make the module to log off the network and allows the firmware to save important data before completely disconnecting from the power supply.

Before the completion of the power-off procedure, the module sends out the URC shown below:

NORMAL POWER DOWN

Since then, no further AT commands or API can be executed. And then the module enters power-down mode, while only RTC is still active.

Refer to ***document [1]*** for details about **AT+QPOWD**.

3.7.2.3. Under-voltage Automatic Shutdown

The module will constantly monitor the voltage applied on VBAT. If the voltage is ≤ 3.6 V, the following URC will be presented:

UNDER_VOLTAGE WARNING

The normal input voltage range is from 3.45 V to 4.25 V. If the voltage is <3.45 V, the module will automatically shut down.

If the voltage is < 3.45 V, the following URC will be presented:

UNDER_VOLTAGE POWER DOWN

Since then, no further AT commands can be executed. The module logs off from network and enters power-down mode, while only RTC is still active.

NOTE

These URCs do not appear when adaptive baud rate is applied and DTE and DCE are not correctly synchronized after start-up. It is recommended to set the module to a fixed baud rate.

3.7.3. Restart the Module

The module can be restart by driving PWRKEY to a low level for a certain time (1-1.2 s), which is similar to the way to turn on module. In order to discharge the internal LDOs completely after turning off the module, it is recommended to delay for about 500 ms before restarting the module. The timing of restarting the module is illustrated as the following figure.

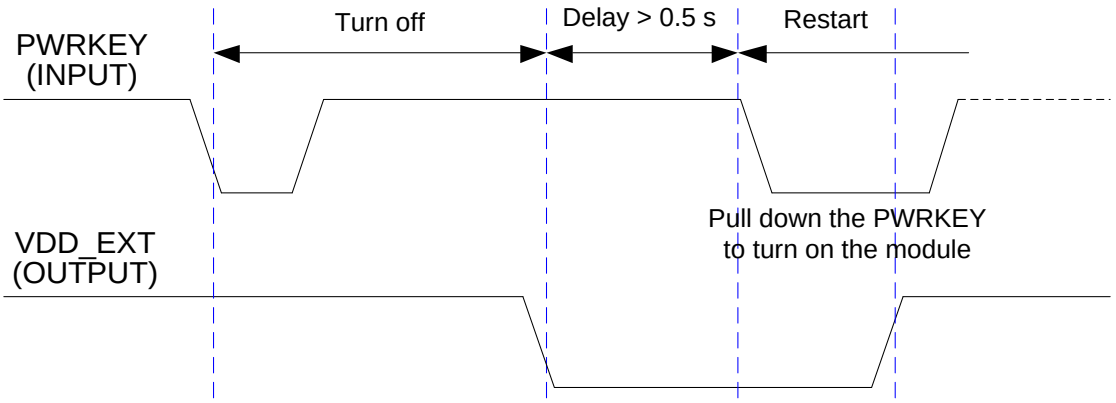

Figure 11: Timing of Restarting the Module

3.8. Power Saving

Based on system requirements, there are two ways to make the module enter a low current consumption status.

- Executing **AT+CFUN=0** to set the module to minimum functionality mode.
- Executing **AT+QSCLK=1** to set the module to sleep mode.

3.8.1. Minimum Functionality Mode

Minimum functionality mode reduces the functionality of the module to a minimum level, and the current consumption can also be minimized when slow clocking mode is activated at the same time. **AT+CFUN** can be used to set module functionality, which provides 3 functionality levels: **<fun>**=0, 1, 4.

- **AT+CFUN=0**: minimum functionality
- **AT+CFUN=1**: full functionality (default)
- **AT+CFUN=4**: disable phone from both transmitting and receiving RF signals

If the module is set by **AT+CFUN=0**, RF and (U)SIM card functions would be disabled. In this case, the UART interface is still accessible, and all AT commands related to RF or (U)SIM card functions will not be available.

If the module is set by **AT+CFUN=4**, RF function would be disabled, but the UART interface is still active. In this case, all AT commands related to RF function would not be available.

For the module already set by **AT+CFUN=0** or **AT+CFUN=4**, **AT+CFUN=1** can be used to set it back to full functionality.

For detailed information about **AT+CFUN**, refer to the ***document [1]***.

3.8.2. Sleep Mode (Slow Clock Mode)

The sleep mode is closed by default. Use **AT+QSCLK=1** or *Ql_SleepEnable()* to make the module enter the sleep mode.

After setting **AT+QSCLK=1**, use DTR pin to allow the module to enter or exit sleep mode. When the DTR pin is set high and no interrupt is generated (such as GPIO interrupt or data transfer occurs in the serial interface), the module will automatically enter the sleep mode. In sleep mode, the module can still receive incoming calls, short messages and GPRS downlink data, but the serial interface is not accessible.

After setting **AT+QSCLK=0**, the module completely exits the sleep mode. At this time, the module will not enter the sleep mode whether DTR is valid or not.

3.8.3. Wake up Module from Sleep Mode

The module can be woken up through the following ways.

- Driving DTR pin for about 800 ms
- Receive a voice or data call from network
- Receive an SMS from network
- External Interrupt
- The timeout of system timer
- Call API function *Ql_SleepDisable()*

NOTE

DTR pin should be held at low level during the communication between the module and DTE.

3.8.4. Mode Transition

Table 8: Mode Transition

Current Mode	Next Mode		
	Power Down	**Normal Mode**	**Sleep Mode**
Power Down	Call the *Ql_PowerDown()* or use the PWRKEY	Use PWRKEY	
Normal Mode	Use **AT+QPOWD** or PWRKEY		Use **AT+QSCLK=1** and drive DTR high
Sleep Mode	Use PWRKEY	Drive DTR low or incoming call/SMS/GPRS data	

3.9. QuecOpen System Reference Design

In order to ensure the stability of the QuecOpen system, it is recommended to use a low-power MCU to monitor the status of the module; the MCU should have a GPIO interface and ADC interface; the system structure diagram is shown in the following figure. This structure has the following two advantages:

- When the ADC detects that the voltage at the VBAT terminal is too low, the MCU will turn off the module through the PWRKEY pin and cut off the power supply through the PMOS transistor.
- During normal operation, the module will output periodic pulses to the MCU. When the MCU does not detect a pulse within the specified time, it will cut off the VBAT power supply and restart the module.

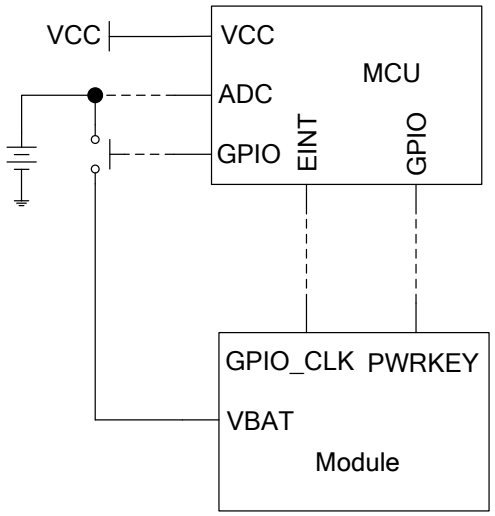

Figure 12: QuecOpen System Reference Design

In addition, the watchdog component can be used to control the power supply of the module. It is recommended to use watchdog components with a timeout of at least 1.6 s, such as the TPS3823-33DBVR model from *Texas Instruments*. Connect a GPIO interface of the module to the WDI pin of the watchdog. If a timeout occurs, the level of the WDI pin will change, and the watchdog will turn off the module. The schematic diagram of watchdog connection is as follows:

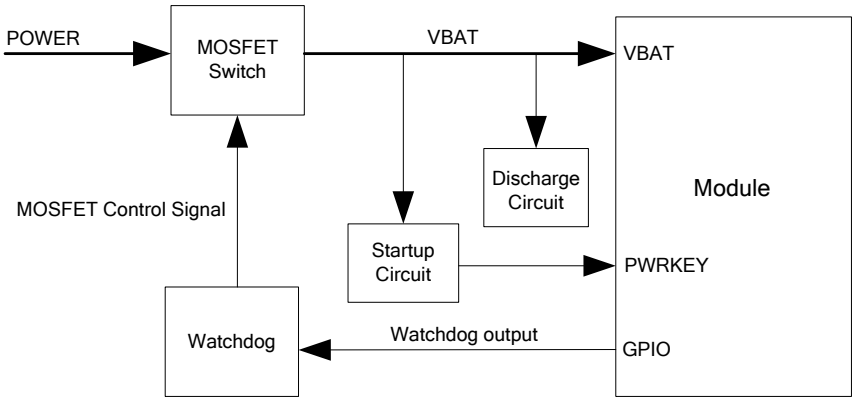

Figure 13: Watchdog Connection Diagram

3.10. RTC Backup Power

The module supports RTC function, and it is designed to work with an internal power supply.

There are three designs for RTC backup power:

- Use VBAT as the power source of RTC.

When the module is turned off while the main power supply (VBAT) is remained, RTC is still active as powered by VBAT. In this case, VRTC pin can be kept open.

- Use VRTC as the power source of RTC.

If the main power supply (VBAT) is removed after the module is turned off, a backup supply, such as a button cell or an ultra-capacitor, can be used to supply power to VRTC pin to keep RTC active.

- Use VBAT and VRTC as the power source of RTC.

It will lead an error of about 5 minutes per day when only the VRTC pin is powered to keep RTC active, therefore, it is recommended to power both VBAT and VRTC pins at the same time when RTC function is needed. The recommended power supply circuits for RTC core are shown below.

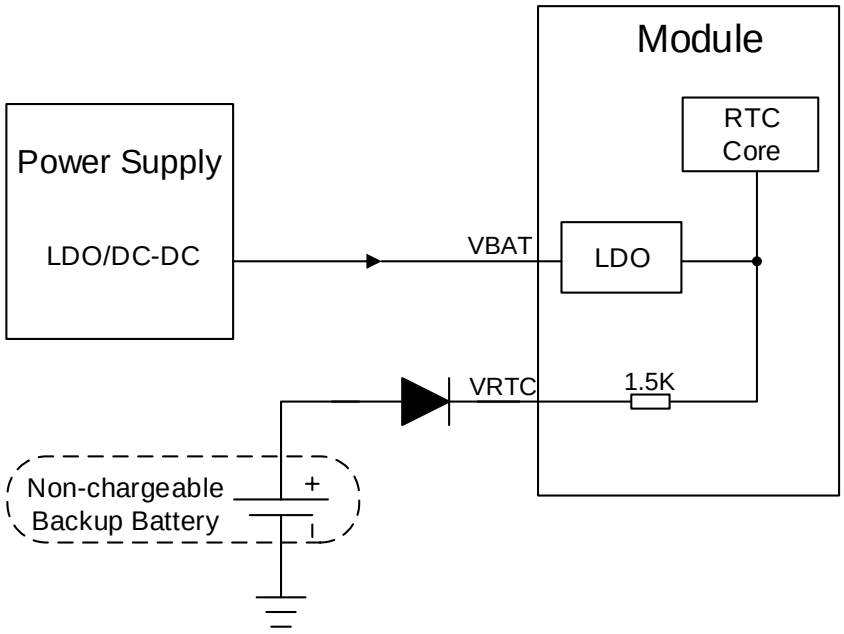

Figure 14: VRTC Supplied by a Non-chargeable Battery

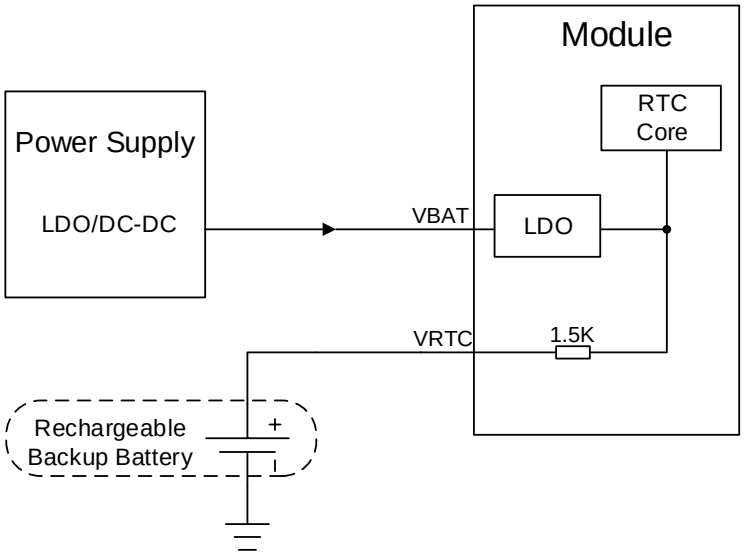

Figure 15: VRTC Supplied by a Rechargeable Battery

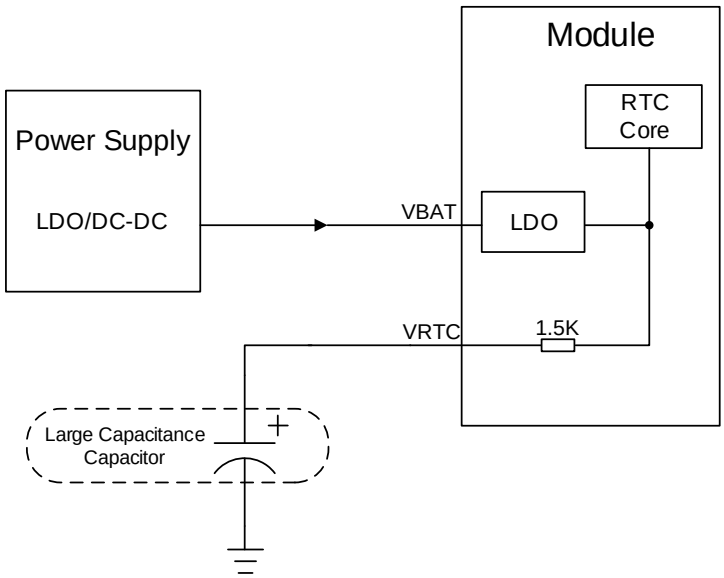

Figure 16: VRTC Supplied by a Capacitor

A rechargeable or non-chargeable coin-cell battery can also be used here, for more information, visit http://www.sii.co.jp/en.

NOTE

Keep the main power supply (VBAT) applied to ensure the accuracy of real-time.

3.11. UART Interfaces

The module provides three UART interfaces: main UART interface, debug UART interface and auxiliary UART interface. The module is designed as a DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection. The supported adaptive baud rate ranges from 4800 bps to 115200 bps.

Pin definition of UART interfaces is as follows:

Table 9: Pin Definition of UART Interfaces

Interface	Pin Name	Pin No.	Description
Main UART Interface	TXD	17	Transmit data
	RXD	18	Receive data
	DTR	19	Data terminal ready
	RI	20	Ring indication
	DCD	21	Data carrier detection
	CTS	22	Clear to send
	RTS	23	Request to send
Debug UART Interface	DBG_RXD	38	Receive data
	DBG_TXD	39	Transmit data
Auxiliary UART Interface	RXD_AUX	28	Receive data
	TXD_AUX	29	Transmit data

Main UART interface:

- TXD: Send data to RXD of DTE.
- RXD: Receive data from TXD of DTE.
- RTS: Request to send.
- CTS: Clear to send.
- DTR: DTE is ready and inform DCE (this pin can wake the module up).
- RI: Ring indication(when there is a call, SMS or URC, the module will inform DTE through RI pin).

- DCD: Data carrier detection (the validity of this pin demonstrates successful set-up of the communication link).

Hardware flow control is disabled by default. When hardware flow control is required, RTS and CTS should be connected to the host. **AT+IFC=2** is used to enable hardware flow control while **AT+IFC=0** is used to disable it. For more details, refer to the ***document [1]***.

Debug UART interface:

- DBG_TXD: Send data to the COM port of peripheral.
- DBG_RXD: Receive data from the COM port of peripheral.

Auxiliary UART interface:

- TXD_AUX: Send data to the RXD of DTE.
- RXD_AUX: Receive data from the TXD of DTE.

Logic levels of UART interfaces are described in the following table.

Table 10: Logic Levels of UART Interfaces

Parameter	Min.	Max.	Unit
V_{IL}	0	0.25 × VDD_EXT	V
V_{IH}	0.75 × VDD_EXT	VDD_EXT + 0.2	V
V_{OL}	0	0.15 × VDD_EXT	V
V_{OH}	0.85 × VDD_EXT	VDD_EXT	V

3.11.1. Main UART Interface

3.11.1.1. Features of Main UART Interface

- Contain data lines TXD and RXD, hardware flow control lines RTS and CTS, as well as other control lines DTR, DCD and RI.
- Used for sending AT command, transmitting GPRS data, etc.
- Support the following baud rates: 2400 bps, 4800 bps, 9600 bps, 14400 bps, 19200 bps, 28800 bps, 38400 bps, 57600 bps and 115200 bps.
- The module is set by default with adaptive baud rate applied in a range of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps and 115200 bps.
- Disable hardware flow control by default. **AT+IFC=2** is used to enable hardware flow control.

Send “**AT**” after a fixed baud rate or adaptive baud rate is set. If the UART interface is ready, “**OK**” will be returned.

Adaptive baud rate is enabled by default. It allows the module to detect the baud rate automatically upon receiving “**AT**” from the host or PC, which offers module flexibility without the needs to consider which baud rate is used by the host controller.

To make full use of adaptive baud rate function, special attention should be paid to the following requirements.

- **Synchronization between DTE and DCE:**

When DCE (the module) is powered on with adaptive baud rate function enabled, it is recommended to wait for 4–5 s before sending the first “**AT**” or “**at**”. If “**OK**” is received, it indicates that DTE and DCE are correctly synchronized.

In the adaptive baud rate mode, If the host controller needs URC, synchronization should be conducted firstly; otherwise, the URC will be discarded.

- **Settings of Adaptive Baud Rate**:

1) The UART interface should be operated at 8 data bits without parity bit or 1 stop bit (factory setting).
2) Only “**AT**” or “**at**” can be detected (“**At**” or “**aT**” cannot be detected).
3) URCs like “**RDY**”, “**+CFUN: 1**” and “**+CPIN: READY**” will not be reported if the module is turned on with adaptive baud rate function enabled while without synchronization conducted at the first time.
4) The module detects the new baud rate upon receiving the first “**AT**” or “**at**”, before this, some other URC will be sent using the previous baud rate. Therefore, DTE may receive undefined characters after switching to new baud rate.
5) It is not recommended to switch to adaptive baud rate mode from fixed baud rates.
6) If an adaptive baud rate is active, it is not recommended to switch to multiplex mode.

NOTE

To assure reliable communication and avoid problems caused by undetermined baud rate between DCE and DTE, it is strongly recommended to configure and save a fixed baud rate instead of using adaptive baud rate after start-up. For more details, refer to the content related to **AT+IPR** in ***document [1]***.

3.11.1.2. Connection for Main UART Interface

The connection between the module and the host using main UART interface is very flexible. The following are three typical connection methods.

The reference design for the full-function UART interface connection is shown below. This connection type is mainly used in modulation demodulation mode

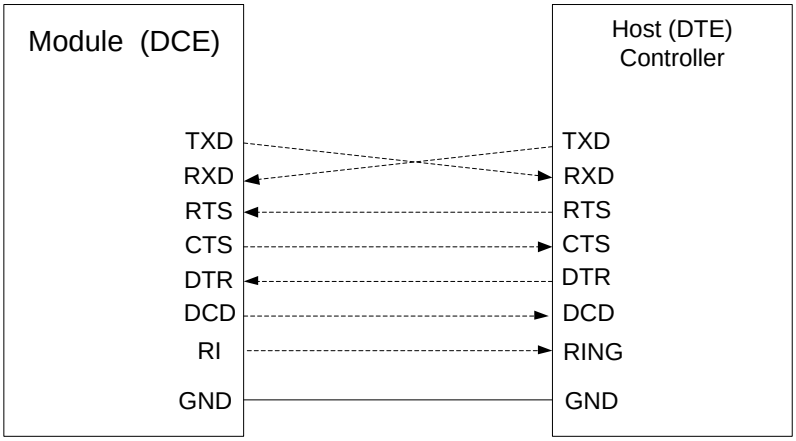

Figure 17: Reference Design for Full-Function UART Interface

Three-wire UART interface connection is shown below.

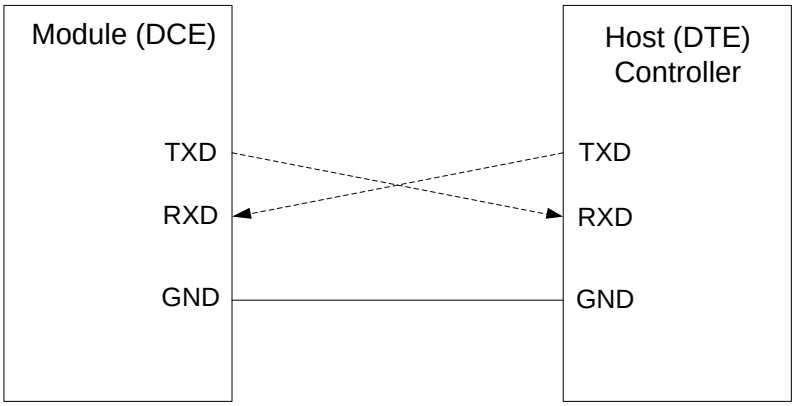

Figure 18: Reference Design for Three-wire UART Interface

The connection for main UART interface with hardware flow control is shown below. This connection will enhance the reliability of the mass data communication.

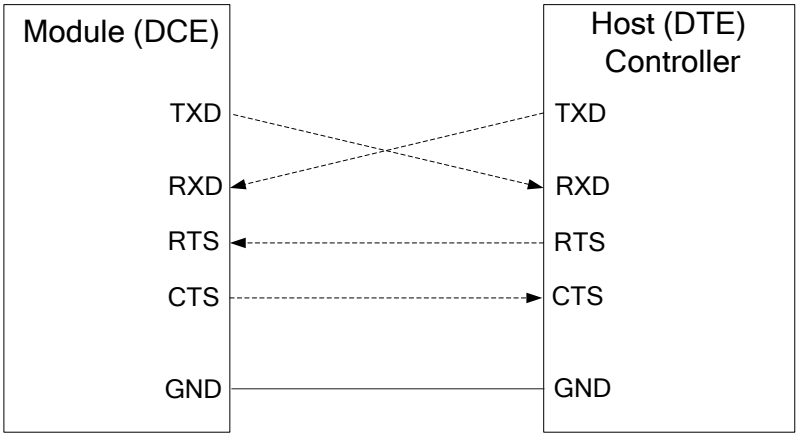

Figure 19: Reference Design for main UART Interface with Hardware Flow Control

3.11.2. Debug UART Interface

- Data lines: DBG_TXD and DBG_RXD.
- It outputs log information automatically.
- It is used for firmware debugging and upgrading with a fixed baud rate of 921600 bps.

During the firmware upgrade process, the PWRKEY pin must be pulled down for more than 1.6 s. The following is a reference design for firmware upgrade.

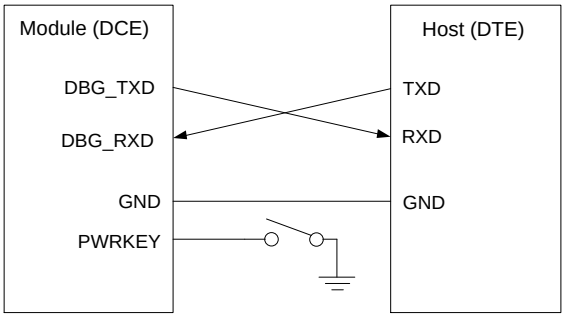

Figure 20: Reference Design for Firmware Upgrade

NOTE

The firmware of the module may need to be upgraded in the future. It is recommended to reserve these pins on the motherboard for firmware upgrade.

3.11.3. Auxiliary UART Interface

- Two data lines: TXD_AUX and RXD_AUX.
- Auxiliary UART interface is used for AT command only and does not support GPRS data, multiplexing function, etc.
- Auxiliary UART interface supports the following baud rates: 2400 bps, 4800 bps, 9600 bps, 14400 bps, 19200 bps, 28800 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps.
- Auxiliary UART interface could be used after sending **AT+QEAUART=1** on main UART interface.
- The baud rate is set as 115200 bps by default, and adaptive baud rate is not supported. The baud rates can be configured by **AT+QSEDCB**. For more details, refer to the ***document [1]***.

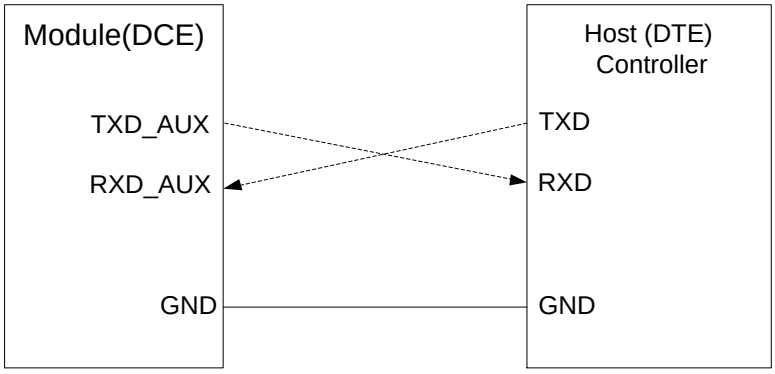

Figure 21: Reference Design for Auxiliary UART Interface

3.11.4. UART Application

The reference design of 3.3 V level match is shown below. If the host is a 3.0 V system, use the 10 kΩ resistor instead of the 5.6 kΩ.

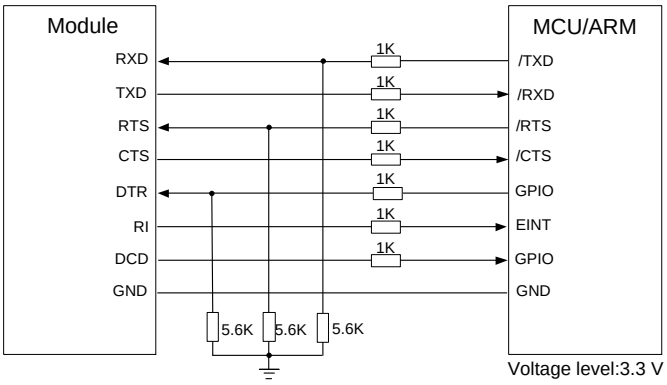

Figure 22: Level Match Design for 3.3 V System

NOTE

If the level of the host is 3.0 V or 3.3 V, it is highly recommended to add resistor divider circuit to the UART signal lines. For higher voltage level system, the level shifter IC could be added between the host and the module. For more details about UART circuit design, refer to ***document [6]***.

When the module communicates with a PC and the level of the module is 2.8 V, a RS-232 level shifter should be used. Make sure that the I/O voltage of level shifter connected to module is 2.8 V. The following figure shows the connection between the module and the standard RS-232 interface.

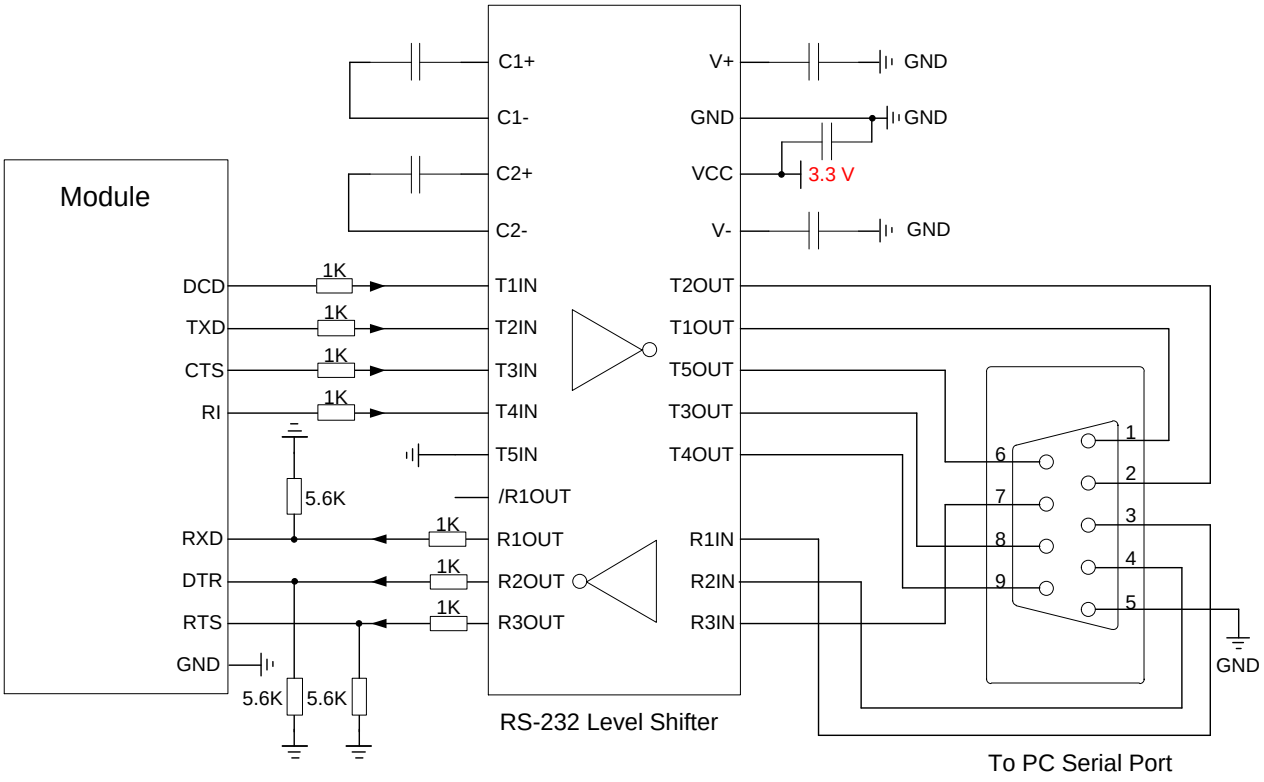

Figure 23: RS-232 Interface Level Shifter Circuit

Visit http://www.maximintegrated.com and http://www.exar.com for more information about RS-232 level shifter IC.

3.12. Audio Interfaces

The module provides one analog input channel and two analog output channels.

Table 11: Pin Definition of Audio Interfaces

Interface	Pin Name	Pin No.	Description
AIN/AOUT1	MICP	3	Microphone input (positive)
	MICN	4	Microphone input (negative)
	SPK1P	5	Audio output Channel 1 (positive)
	SPK1N	6	Audio output Channel 1 (negative)
AIN/AOUT2	MICP	3	Microphone input (positive)
	MICN	4	Microphone input (negative)
	SPK2P	2	Audio output Channel 2 (positive)
	AGND	1	Form a pseudo-differential pair with SPK2P

The AIN is a differential input channel that can be used for the input of the microphone (usually using an electret microphone).

AOUT1 is used for the output of receiver. It is a differential channel that typically applied for building a receiver into a handset.

AOUT2 is a single-ended channel that typically used for headset. SPK2P and AGND can form a pseudo-differential structure.

All these audio channels support voice and ringtone output, etc., and can be switched to each other by **AT+QAUDCH**. For more details, refer to ***document [1]***.

Use **AT+QAUDCH** to select audio channel:

- **AT+QAUDCH=0**: AIN/AOUT1, 0 is by default.
- **AT+QAUDCH=1**: AIN/AOUT2, this channel is always used for headset.

For each channel, it is suggested to use **AT+QMIC** to adjust the microphone gain level and **AT+CLVL** to adjust the loud speaker volume level. **AT+QSIDET** is used to set the side tone gain level. For more details, refer to ***document [1]***.

3.12.1. Decrease TDD Noise and Other Noises

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied to filter out 900 MHz RF interference when the module is transmitting at EGSM900MHz, and without placing this capacitor,

TDD noise could be heard; while the 10 pF capacitor is used to filter out 1800 MHz RF interference. Note that the frequency resonant point of a capacitor largely depends on the material and production technique. Therefore, you should discuss with capacitor vendors to choose the most suitable capacitors for filtering out RF interference when the module is working at GSM850MHz, EGSM900MHz, DCS1800MHz and PCS1900MHz separately.

The severity degree of the RF interference in the audio channel during GSM transmission process largely depends on the application design. Therefore, you can choose a suitable capacitor based on the test results. Sometimes, even no RF filtering capacitor is required.

The capacitor which is used for filtering out RF interference should be close to the audio interface, and the audio trace should be as short as possible.
In order to decrease radio or other signal interference, the RF antenna should be placed away from audio interface and trace. The power trace should not be parallel with or close to the audio trace.

The differential audio traces must be routed according to the differential signal layout principles.

3.12.2. Microphone Interface Design

AIN channels have internal bias supply voltage for external electret microphone. A reference circuit is shown in the following figure.

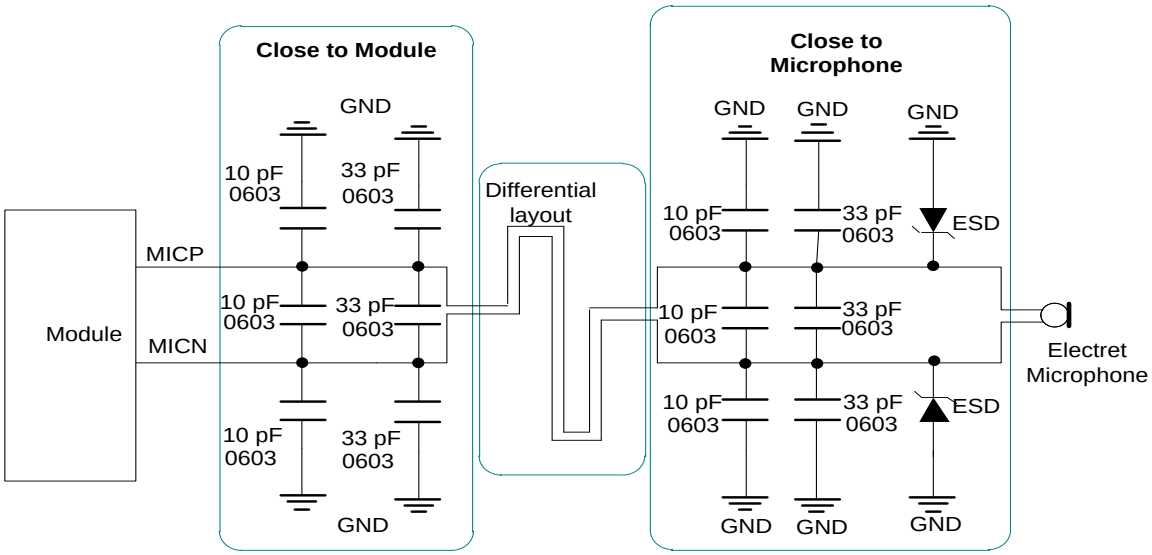

Figure 24: Reference Design for Microphone Interface

3.12.3. Speaker Interface Design

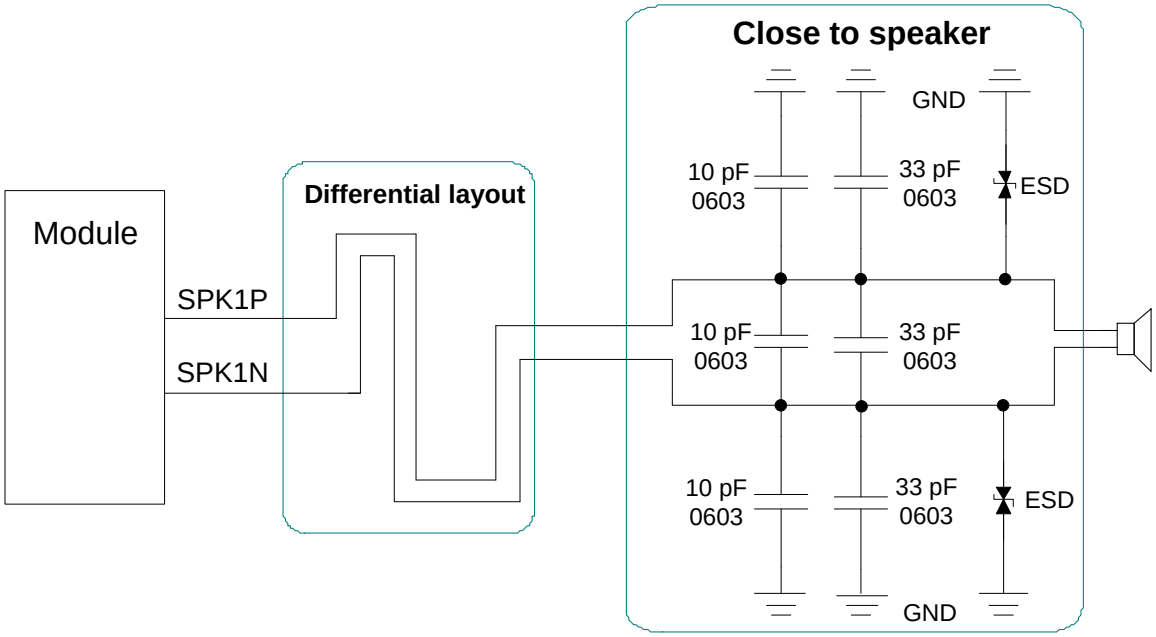

Figure 25: Reference Design for Speaker Interface

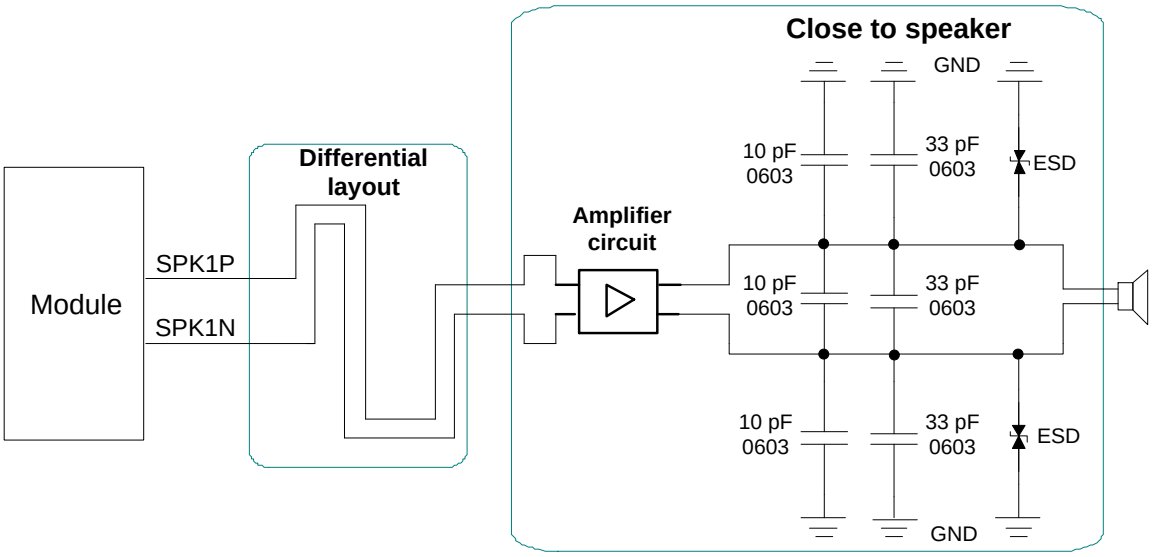

Figure 26: Reference Design for Speaker with an Amplifier

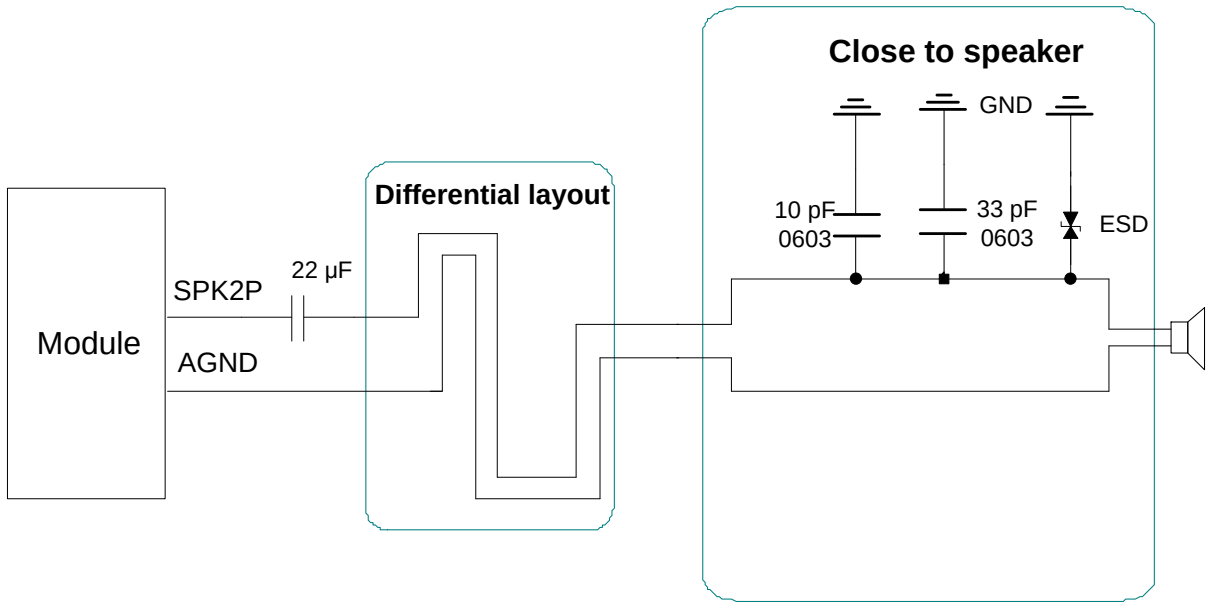

Figure 27: Reference Design for Headset Interface for AOUT2

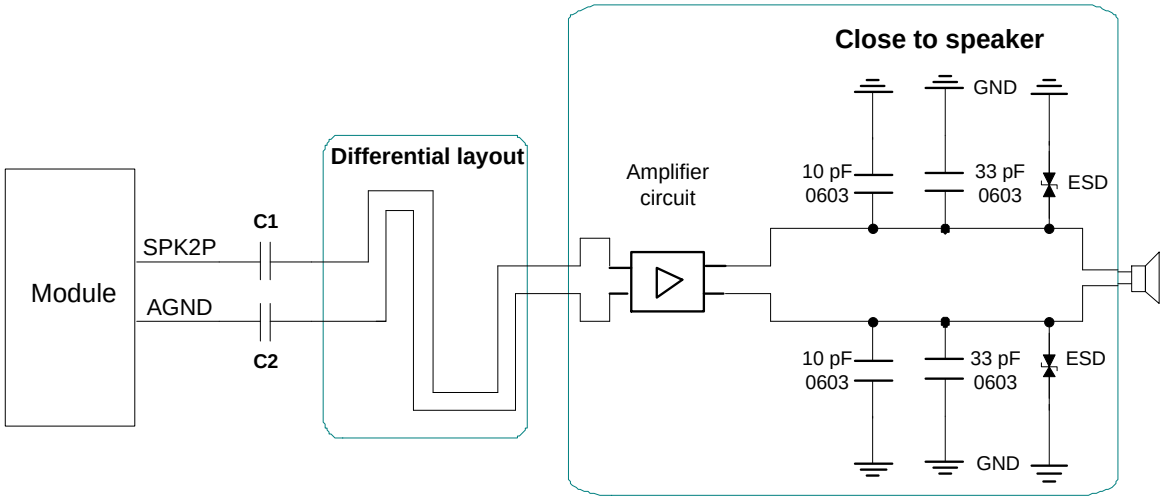

Figure 28: Reference Design for Speaker with an Amplifier for AOUT2

Visit http://www.ti.com for more information about differential audio amplifiers.

NOTE

The value of C1 and C2 here depends on the input impedance of audio amplifier.

3.12.4. Headset Interface Design

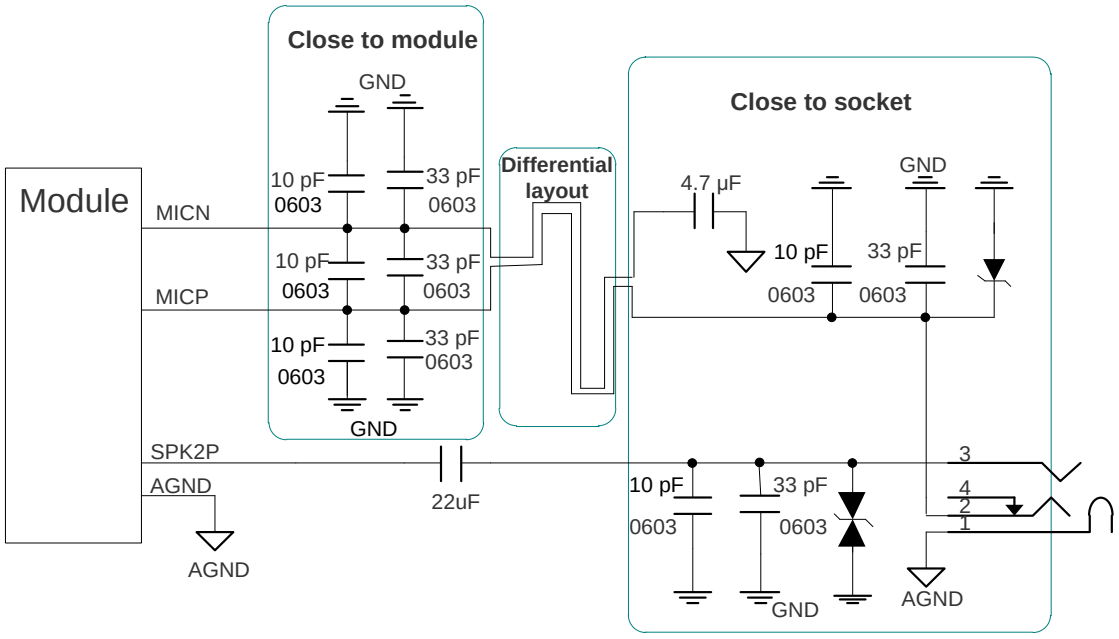

Figure 29: Reference Design for Headset Interface

3.12.5. Audio Characteristics

Table 12: Typical Characteristics of Electret Microphone

Parameter	Min.	Typ.	Max.	Unit
Working Voltage	1.8	2	2.4	V
Working Current			1000	µA
External Microphone Load Resistance	2			kΩ

Table 13: Typical Characteristics of Speaker

Parameter			Min.	Typ.	Max.	Unit
AOUT1 Output	Single-ended	Load resistance		32		Ω
		Reference level	0		1.85	Vpp
	Differential	Load resistance		32		Ω
		Reference level	0		3.7	Vpp
AOUT2 Output	Single-ended	Load resistance		32		Ω
		Reference level	0		0.92	Vpp

3.13. I2C Interface

The I2C interface supports the multiplexing function of the RI and DCD pins; the corresponding two signal lines are SCL and SDA. The main features of the I2C interface are as follows:

- Support host mode
- Support adjustable clock frequency in LS/FS mode
- Support 7-bit addressing mode
- Support high speed mode

Table 14: The Logic Level of I2C Interface

Parameter	Min.	Max.	Unit
V_{IL}	0	0.25 × VDD_EXT	V
V_{IH}	0.75 × VDD_EXT	VDD_EXT + 0.2	V
V_{OL}	0	0.15 × VDD_EXT	V
V_{OH}	0.85 × VDD_EXT	VDD_EXT	V

3.14. (U)SIM Interface

The (U)SIM interface is compliant with the GSM Phase 1 specification and the new GSM Phase 2+ specification, and supports FAST 64 kbps (U)SIM card (applicable to (U)SIM application toolkit).

The (U)SIM interface is powered by an internal regulator in the module. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 15: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	Description	Multiplexing Function [1)]
SIM_VDD	14	● Supply power for (U)SIM card ● Automatically detect (U)SIM card voltage ● 3.0 V ±5% and 1.8 V ±5% ● Maximum supply current is about 10 mA	
SIM_CLK	13	(U)SIM card clock	
SIM_DATA	11	(U)SIM card data	
SIM_RST	12	(U)SIM card reset	
SIM_GND	10	(U)SIM card ground	
SIM_PRESENCE	19	(U)SIM card insertion detection	DTR

NOTE

[1)] If several interfaces share the same I/O pin, only one peripheral can be enabled at a time to avoid conflict between these multiplexing functions.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

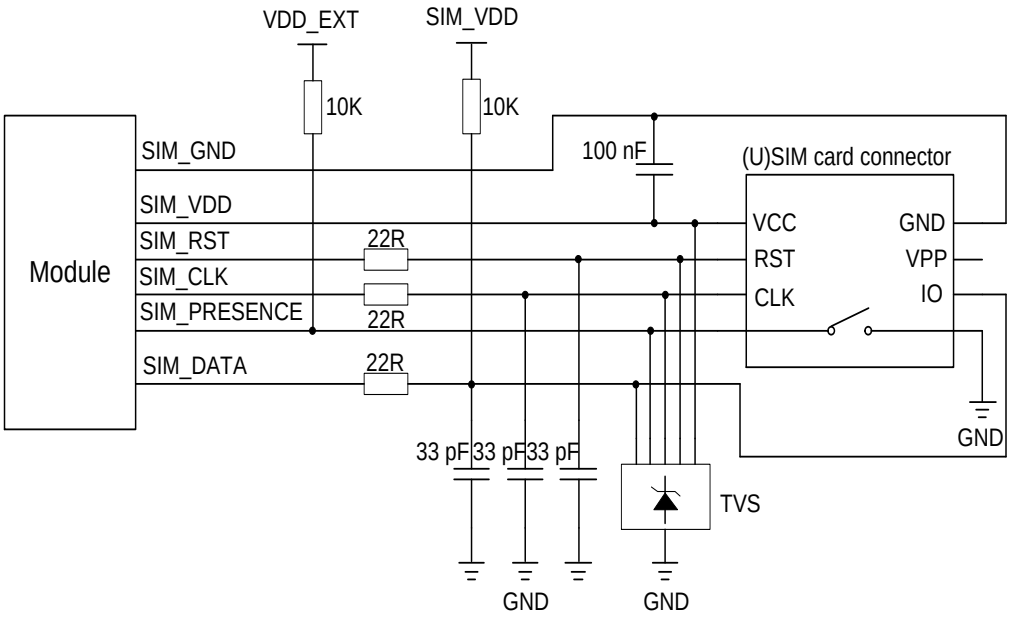

Figure 30: Reference Design for (U)SIM Interface with the 8-pin (U)SIM Card Connector

If (U)SIM card insertion detection function is not used, keep SIM_PRESENCE pin unconnected. A reference design for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

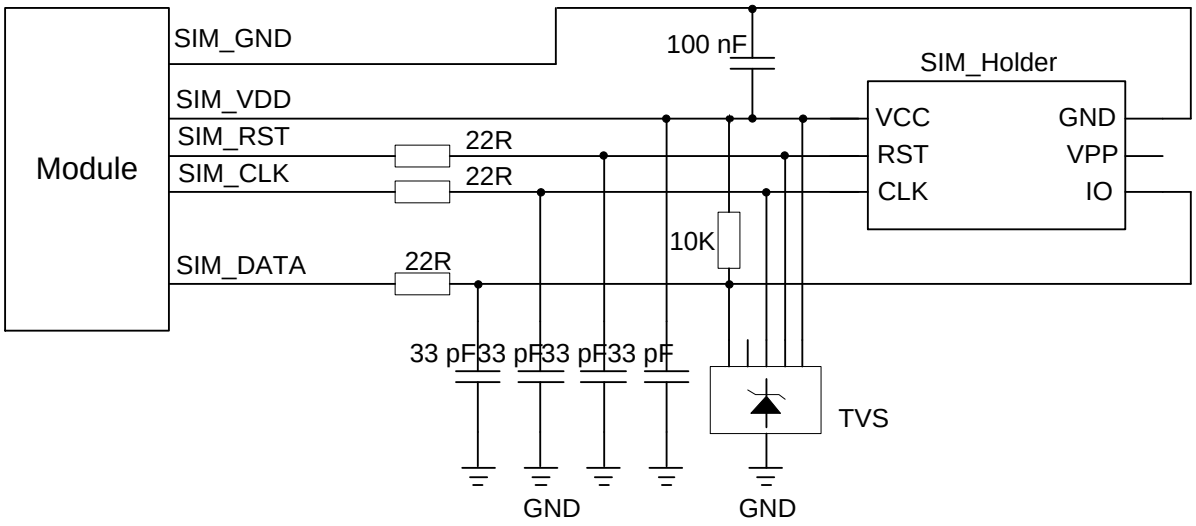

Figure 31: Reference Design for (U)SIM Interface with the 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in application, follow the criteria below in the (U)SIM circuit design:

- Place the (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make the ground between module and (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to avoid any decrease in electric potential. The bypass capacitor between SIM_VDD and SIM_GND should be no more than 1 μF and be placed close to the (U)SIM card connector.
- To avoid cross-talk between SIM_DATA and SIM_CLK, keep them away from each other and shield them separately with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should be no more than 50 pF. The ESD protection device should be placed close to (U)SIM card connector, and make sure the (U)SIM card signal lines go through the ESD protection device from (U)SIM card connector first and then to the module. The 22 Ω resistors should be connected in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on SIM_DATA line can improve anti-jamming capability in sensitive occasions or when long traces are applied, and should be placed close to the (U)SIM card connector.

3.15. ADC Interface

The module provides an ADC interface to read the voltage value. You can execute **AT+QADC=1** to read the voltage value on ADC0. For details of this AT command, refer to the ***document [1]*.**

To improve the accuracy of ADC, the layout of ADC should be surrounded by ground.

Table 16: Pin Definition of ADC Interface

Pin Name	Pin No.	Description
AVDD	8	Reference voltage of ADC circuit
ADC0	9	General-purpose ADC Interface

Table 17: Characteristics of ADC

Parameter	Min.	Typ.	Max.	Unit
Voltage Range	0		1.8	V
ADC Resolution		10		bits

ADC Accuracy	2.7	mV

3.16. RI Behaviors

Table 18: RI Behaviors

State	RI Response
Standby	HIGH
Voice call	Change to LOW, then: 1. Change to HIGH when a call is established. 2. Use **ATH** to hang up the call; RI changes to HIGH. 3. Caller hangs up, RI changes to HIGH first, and changes to LOW for 120 ms indicating URC "**NO CARRIER**", then changes to HIGH again. 4. Change to HIGH when SMS is received.
SMS	When there is a new SMS, RI changes to LOW and holds for about 120 ms, then it changes to HIGH.
URC	Certain URCs can keep RI LOW for 120 ms.

If the module is used as a caller, RI would remain in HIGH except URC or SMS is received.

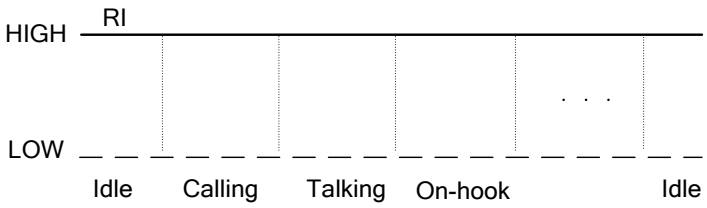

Figure 32: RI Timing As a Caller

On the other hand, when it is used as a receiver, the timing of RI is shown below.

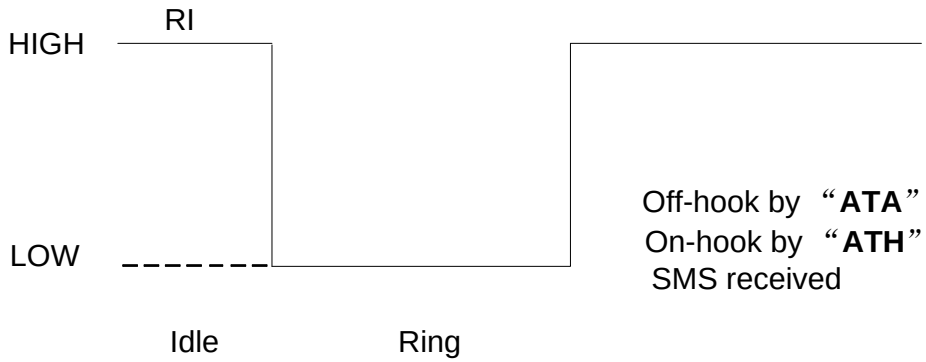

Figure 33: RI Timing As a Receiver

When URC or SMS is received, the timing of RI is shown below.

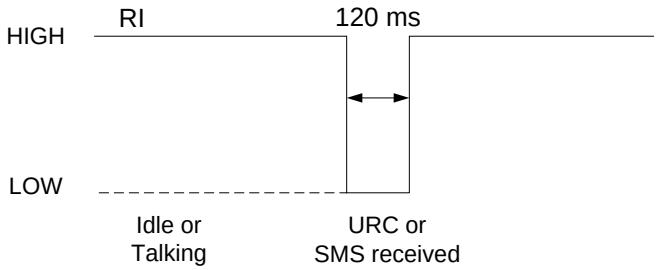

Figure 34: RI Timing When a URC or SMS is Received

3.17. Network Status Indication

The NETLIGHT signal can be used to indicate the network status of the module. The following table illustrates the module status indicated by NETLIGHT.

Table 19: Module Status Indicated by NETLIGHT

NETLIGHT Level	Module Status
Always Low (LED Off)	The module is not working or the modem is in idle/PSM mode.
64 ms High (LED On)/800 ms Low (LED Off)	The module is not synchronized with network.
64 ms High (LED On)/2000 ms Low (LED Off)	The module is synchronized with network.
64 ms High (LED On)/600 ms Low (LED Off)	GPRS data transmission upon PPP dial-up connection.

A reference design is shown as below.

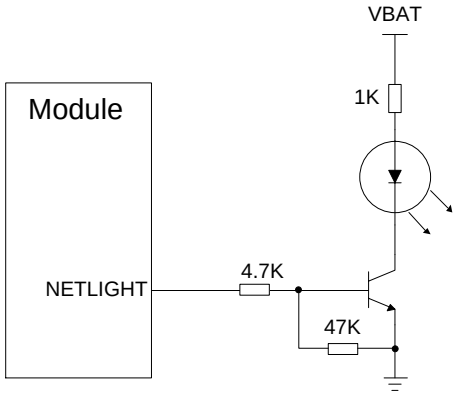

Figure 35: Reference Design for NETLIGHT

3.18. RF Transmitting Signal Indication

The module provides a RFTXMON pin which will output a high level when the GSM transmitter is active and low level when transmitting activity is completed.

Table 20: Pin Definition of RFTXMON

Pin Name	Pin No.	Description
RFTXMON	25	Transmission signal indication

There are two different modes for this function:

1) Active during the transmitting activity

RFTXMON is used to indicate the transmit burst. If it outputs a high level, there will be a transmit burst of 220 μs later.

AT+QCFG="RFTXburst",1 can be executed to enable the function.

The timing of the RFTXMON signal is shown below.

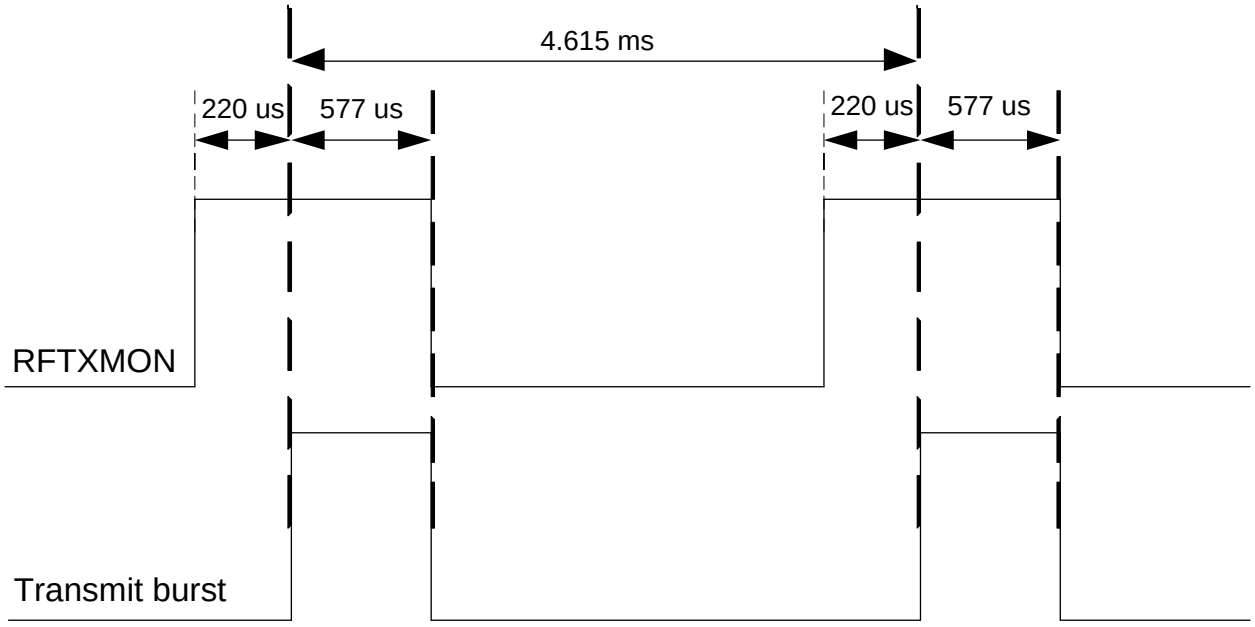

Figure 36: RFTXMON Signal During Burst Transmission

2) Active during the call

RFTXMON will output a high level during a call and the pin will output a low level after being hanged up.

AT+QCFG="RFTXburst",2 can be executed to enable the function.

The timing of the RFTXMON signal is shown below.

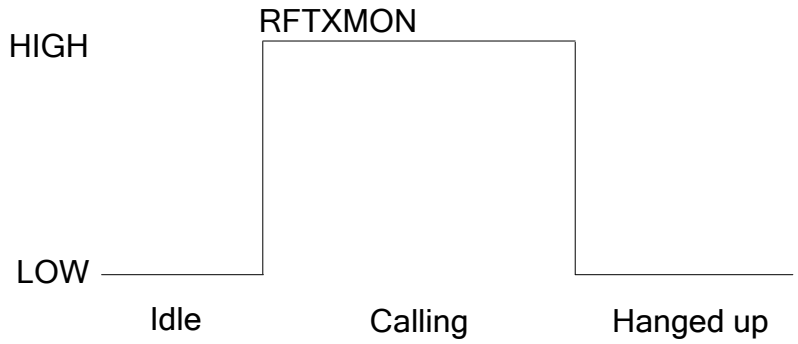

Figure 37: RFTXMON Signal During Call

3.19. GPIO Interfaces

The module provides 13 GPIO interfaces. To reduce the number of pins, some GPIO interfaces can be multiplexed; when the default functions of these pins are not used, they can be configured as GPIO. GPIO can be configured through API functions, such as *Ql_GPIO_Init()*, *Ql_GPIO_SetLevel()*, *Ql_GPIO_SetDirection()* and *Ql_GPIO_SetPullSelection()*. For more details about these API functions, refer to ***document [14].***

Table 21: GPIO Interfaces List

Pin Name	Pin No.	Mode	Reset		Mode 4
			I/O	PU/PD/OFF	
NETLIGHT	16	Mode 2	O	OFF	4 mA
DTR	19	Mode 2	I	PD	4 mA
RI	20	Mode 2	O	OFF	4 mA
DCD	21	Mode 2	O	OFF	4 mA
CTS	22	Mode 2	I	PD	4 mA
RTS	23	Mode 2	I	PD	4 mA
RFTXMON	25	Mode 2	I	PD	4 mA
RXD_AUX	28	Mode 2	I	PD	4 mA
TXD_AUX	29	Mode 2	I	PD	4 mA
PCM_CLK	30	Mode 2	O	OFF	4 mA
PCM_SYNC	31	Mode 2	O	OFF	4 mA
PCM_IN	32	Mode 2	O	OFF	4 mA
PCM_OUT	33	Mode 2	O	PD	4 mA

NOTE

- O: Output;
- I: Input;
- PU: Pull-up;
- PD: Pull-down;
- OFF: Pull-up and pull-down are not allowed by default.

3.20. External Interrupt

All pins of the module that can be reused as GPIO have an external interrupt function, which is also a multiplexed function. When the default function of the related pin is not used, it can be configured as an external interrupt.

4 Antenna Interface

4.1. GSM Antenna Interface

M65 QuecOpen has a GSM antenna interface with an impedance of 50 Ω.

The pin definition of GSM antenna interface is as follows:

Table 22: Pin Definition of GSM Antenna Interface

Pin Name	Pin No.	Description
RF_ANT	35	GSM antenna pin
GND	34, 36, 37	Ground

4.1.1. Reference Design

The external antenna must be matched properly to achieve the best performance, so the matching circuit should be reserved. The reference design for GSM antenna is shown below, among which C1 and C2 are should not be mounted and only the R1 should be mounted.

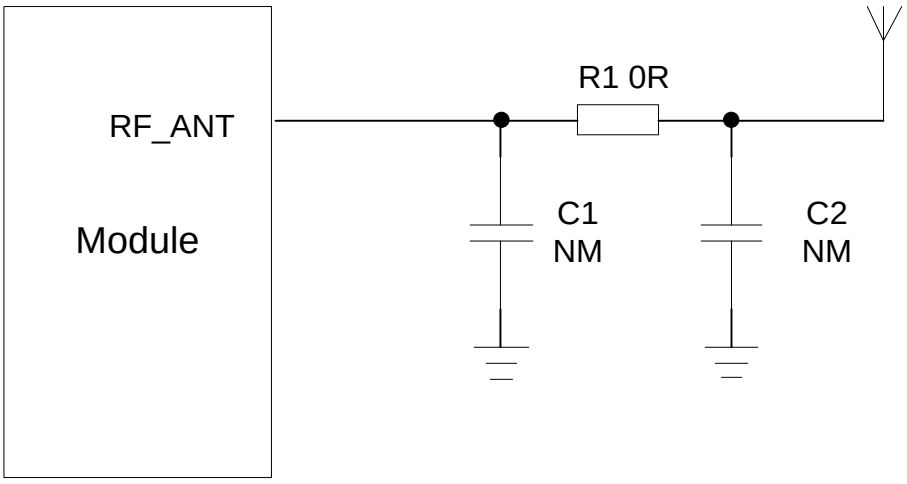

Figure 38: Reference Design for GSM Antenna

M65 QuecOpen provides an RF antenna pin for antenna connection. The RF trace in host PCB connected to the module RF antenna pin should be coplanar waveguide line or microstrip line, whose characteristic impedance should be close to 50 Ω. M65 QuecOpen comes with grounding pins which are next to the antenna pin in order to give a better grounding. Besides, a π type match circuit is recommended to be used to adjust the RF performance.

To minimize the loss on RF trace and RF cable, take design into account carefully. The following table shows the requirement on the GSM antenna.

Table 23: Antenna Cable Requirements

Frequency	Requirements
GSM850/EGSM900	Cable insertion loss < 1 dB
DCS1800/PCS1900	Cable insertion loss < 1.5 dB

Table 24: Antenna Requirements

Type	Requirements
Frequency Range	GSM850/EGSM900/DCS1800/PCS1900
VSWR	≤ 2
Gain (dBi)	1
Max. Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Vertical

4.1.2. RF Output Power

Table 25: RF Output Power

Frequency	Max.	Min.
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB

PCS1900	30 dBm ±2 dB	0 dBm ±5 dB

4.1.3. RF Receiving Sensitivity

Table 26: RF Receiving Sensitivity

Frequency	Receiving Sensitivity
GSM850	< -108 dBm
EGSM900	< -108 dBm
DCS1800	< -107 dBm
PCS1900	< -107 dBm

4.1.4. Operating Frequencies

Table 27: Operating Frequencies

Frequency	Receive	Transmit	ARFCH
GSM850	869–894 MHz	824–849 MHz	128–251
EGSM900	925–960 MHz	880–915 MHz	0–124, 975–1023
DCS1800	1805–1880 MHz	1710–1785 MHz	512–885
PCS1900	1930–1990 MHz	1850–1910 MHz	512–810

4.1.5. RF Cable Soldering

Soldering RF cable to RF pin of module in a correct way will reduce the loss on the path of RF, refer to the following example of RF soldering.

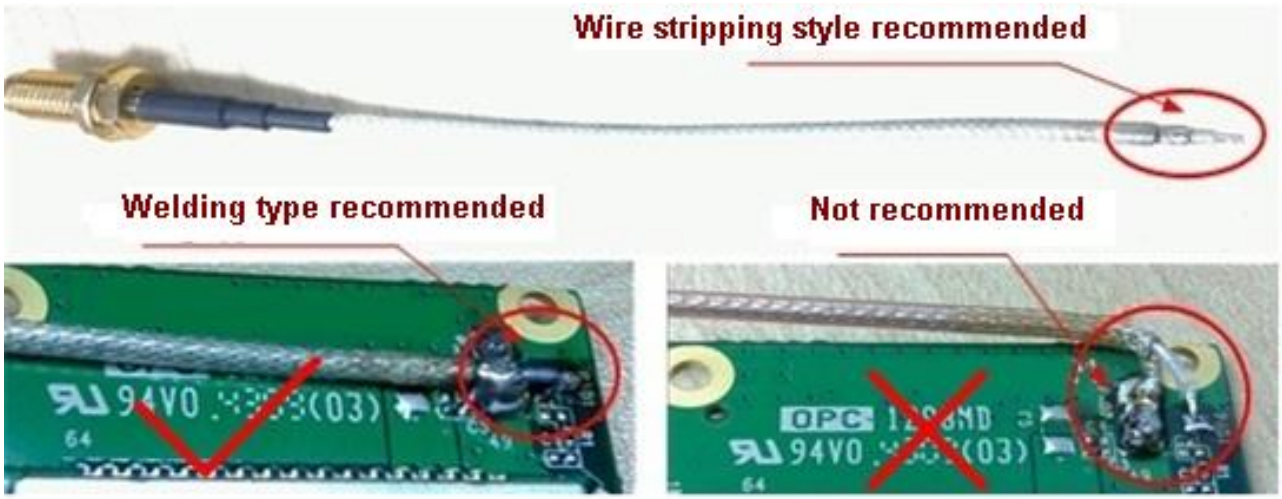

Figure 39: RF Soldering Sample

5 Reliability, Radio and Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 28: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	+4.5	V
Peak Current of Power Supply	0	2.0	A
RMS Current of Power Supply (during one TDMA-frame)	0	0.7	A
Voltage at Digital Pins	-0.3	3.08	V
Voltage at Analog Pins	-0.3	3.08	V

5.2. Operating and Storage Temperatures

The following table lists the operating and storage temperatures of the module.

Table 29: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [1)]	-35	+25	+75	°C
Extended temperature range [2)]	-40		+85	°C

Storage Temperature Range	-40	+90	°C

NOTE

1. [1] Within the operating temperature range, the module is 3GPP compliant.
2. [2] Within the extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There won't be unrecoverable malfunctions. Nor will there be effects on the radio spectrum or harm to the radio network. Only one or more parameters like P_{out} might reduce in the value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

5.3. Power Supply Ratings

Table 30: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	Supply voltage	The actual input voltages must stay between the minimum and maximum values	3.45	4.0	4.25	V
	Voltage drop during burst transmission	Maximum power control level on GSM850 and EGSM900			400	mV
I_{VBAT}	Average supply current	Power down mode		39		μA
		Sleep mode @DRX=5		1.2		mA
		Minimum functionality mode				
		● **AT+CFUN=0**				
		Idle mode		9.5		mA
		Sleep mode		0.8		mA
		● **AT+CFUN=4**				
		Idle mode		9.5		mA
		Sleep mode		0.8		mA
		Talk mode				
		GSM850/EGSM900 [1]		241/229		mA
		DCS1800/PCS1900 [2]		178/156		mA
		Data mode, GPRS (3 Rx, 2 Tx)				
		GSM850/EGSM900 [1]		366/343		mA
		DCS1800/PCS1900 [2]		251/222		mA
		Data mode, GPRS (2 Rx, 3 Tx)				
		GSM850/EGSM900 [1]		423/397		mA

		DCS1800/PCS1900 [2]	283/254		mA
		Data mode, GPRS (4 Rx, 1 Tx) GSM850/EGSM900 [1] DCS1800/PCS1900 [2]	 234/221 165/149		 mA mA
		Data mode, GPRS (1 Rx, 4 Tx) GSM850/EGSM900 [1] DCS1800/PCS1900 [2]	 457/437 315/283		 mA mA
	Peak supply current (during transmission slot)	Maximum power control level on GSM850 and EGSM900	1.8	2	A

NOTE

1. [1] Power control level PCL 5.
2. [2] Power control level PCL 0.

5.4. Current Consumption

Table 31: Current Consumption

Condition	Current Consumption
Voice Call	
GSM850	@power level #5, < 300 mA, Typ. 241 mA @power level #12, Typ. 103 mA @power level #19, Typ. 73 mA
EGSM900	@power level #5, < 300 mA, Typ. 229 mA @power level #12, Typ. 102 mA @power level #19, Typ. 74 mA
DCS1800	@power level #0, < 250 mA, Typ. 177 mA @power level #7, Typ. 87 mA @power level #15, Typ. 68 mA
PCS1900	@power level #0, < 250 mA, Typ. 156 mA @power level #7, Typ. 85 mA @power level #15, Typ. 67 mA
GPRS Data	
DATA Mode, GPRS (3 Rx, 2 Tx) Class 12	

GSM850	@power level #5, < 550 mA, Typ. 366 mA
EGSM900	@power level #5, < 550 mA, Typ. 343 mA
DCS1800	@power level #0, < 450 mA, Typ. 251 mA
PCS1900	@power level #0, < 450 mA, Typ. 222 mA
DATA Mode, GPRS (2 Rx, 3 Tx) Class 12	
GSM850	@power level #5, < 640 mA, Typ. 423 mA
EGSM900	@power level #5, < 600 mA, Typ. 397 mA
DCS1800	@power level #0, < 490 mA, Typ. 283 mA
PCS1900	@ power level #0, < 490 mA, Typ. 254 mA
DATA Mode, GPRS (4 Rx,1 Tx) Class 12	
GSM850	@power level #5, < 350 mA, Typ. 234 mA
EGSM900	@power level #5, < 350 mA, Typ. 221 mA
DCS1800	@power level #0, < 300 mA, Typ. 165 mA
PCS1900	@power level #0, < 300 mA, Typ. 149 mA
DATA Mode, GPRS (1 Rx, 4 Tx) Class 12	
GSM850	@power level #5, <660 mA, Typ. 453 mA
EGSM900	@power level #5, <660 mA, Typ. 437 mA
DCS1800	@power level #0, <530 mA, Typ. 315 mA
PCS1900	@power level #0, <530 mA, Typ. 283 mA

NOTE

GPRS Class 12 is the default setting. The module can be configured from GPRS Class 1 to Class 12 via **AT+QGPCLASS**. When it is set to a lower GPRS class, the power consumption of the module will be lower as well.

5.5. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of the module.

Table 32: Electrostatic Discharge Characteristics (25ºC, 45% Relative Humidity)

Tested Point	Contact Discharge	Air Discharge
VBAT, GND	±5 kV	±10 kV
RF_ANT	±5 kV	±10 kV
TXD, RXD	±2 kV	±4 kV
Others	±0.5 kV	±1 kV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions of the Module

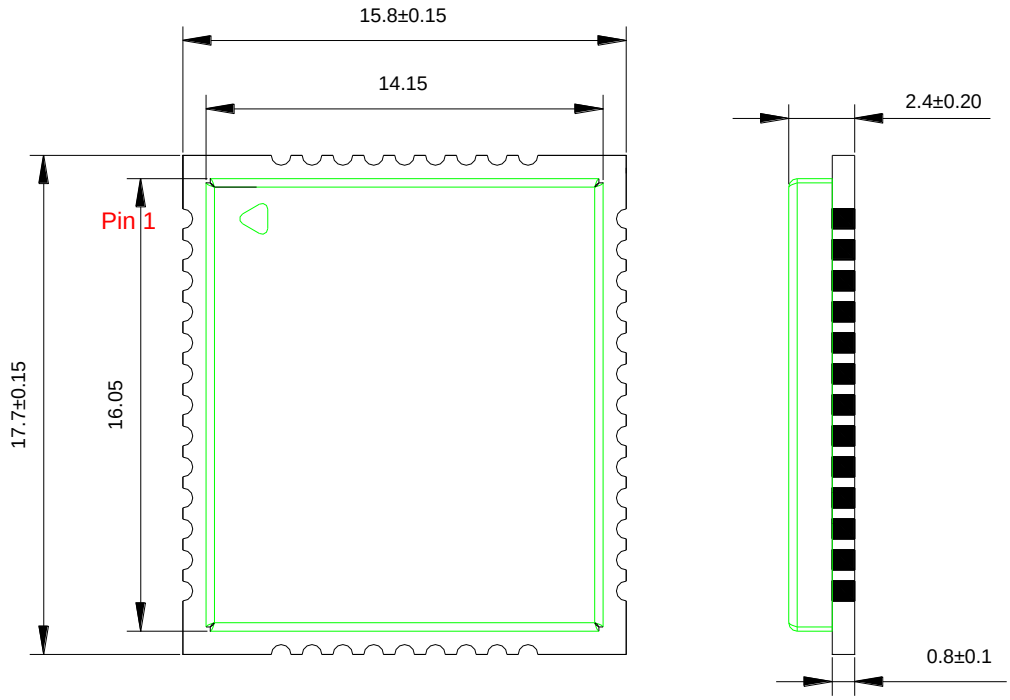

Figure 40: Module Top and Side Dimensions

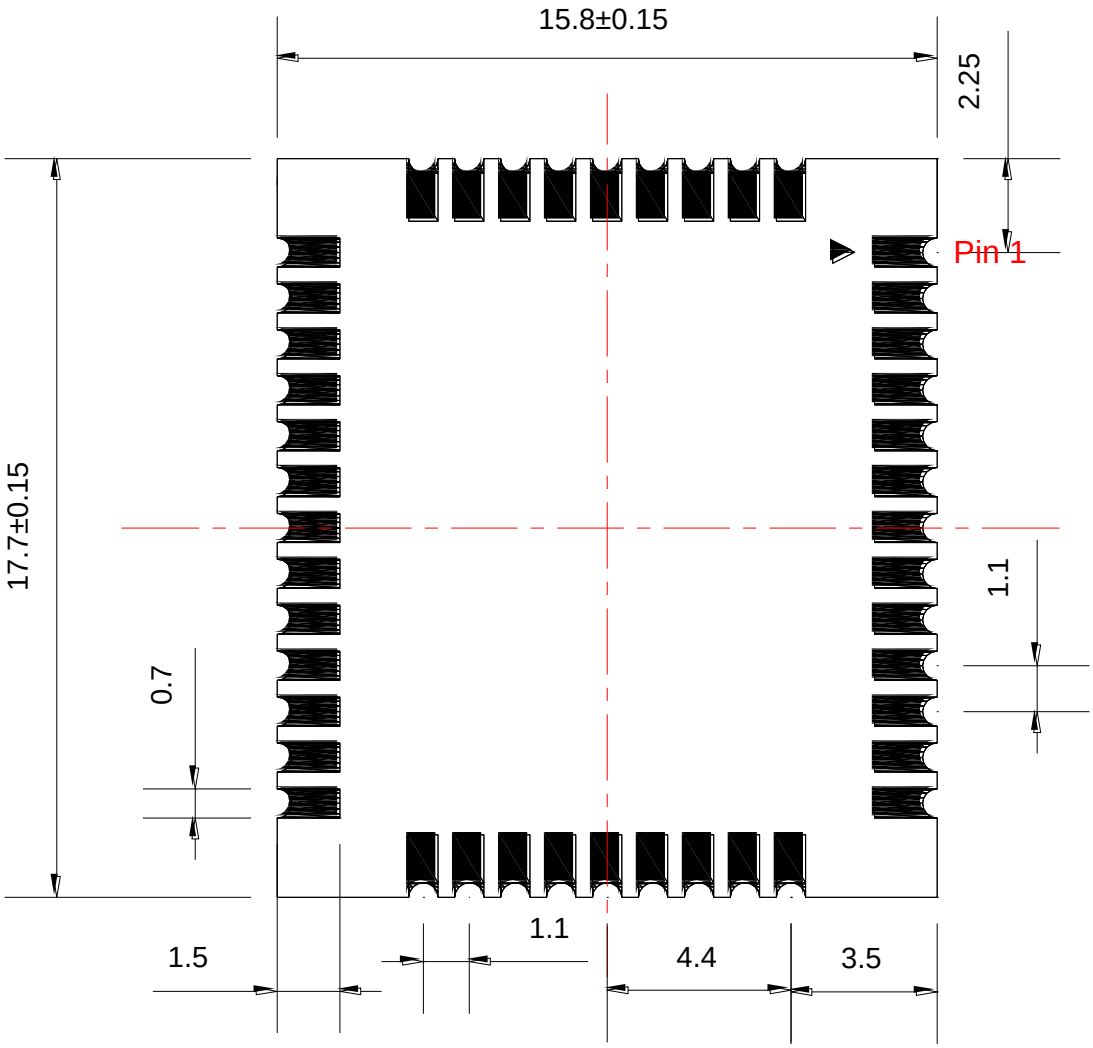

Figure 41: Module Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

6.2. Recommended Footprint

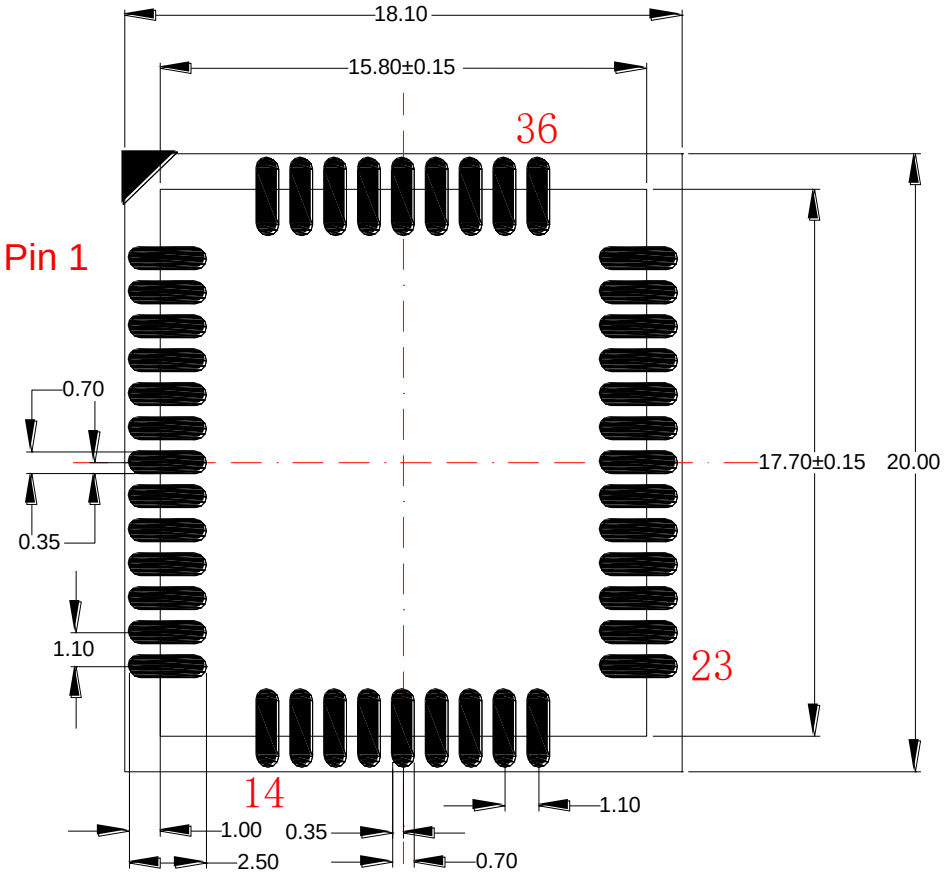

Figure 42: Recommended Footprint (Top View)

NOTE

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the motherboard.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm.

6.3. Top and Bottom Views of the Module

Figure 43: Top View of the Module

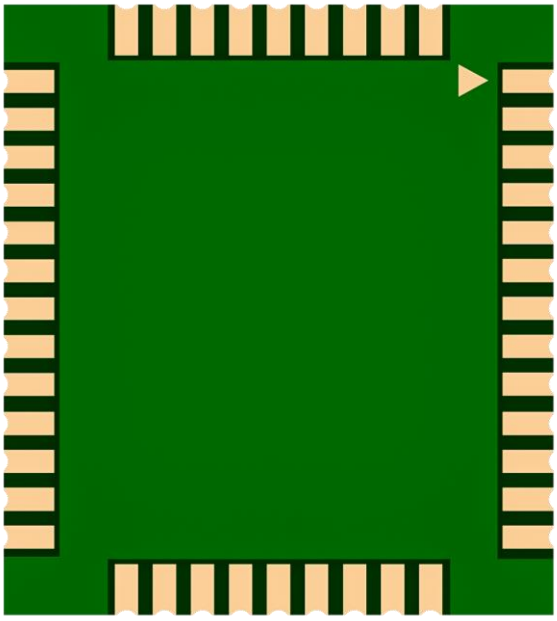

Figure 44: Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTE

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60 %, it is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Take the module out of the packaging and put it on high-temperature resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, refer to ***document [5]***.

It is suggested that the peak reflow temperature is 235 ºC to 246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

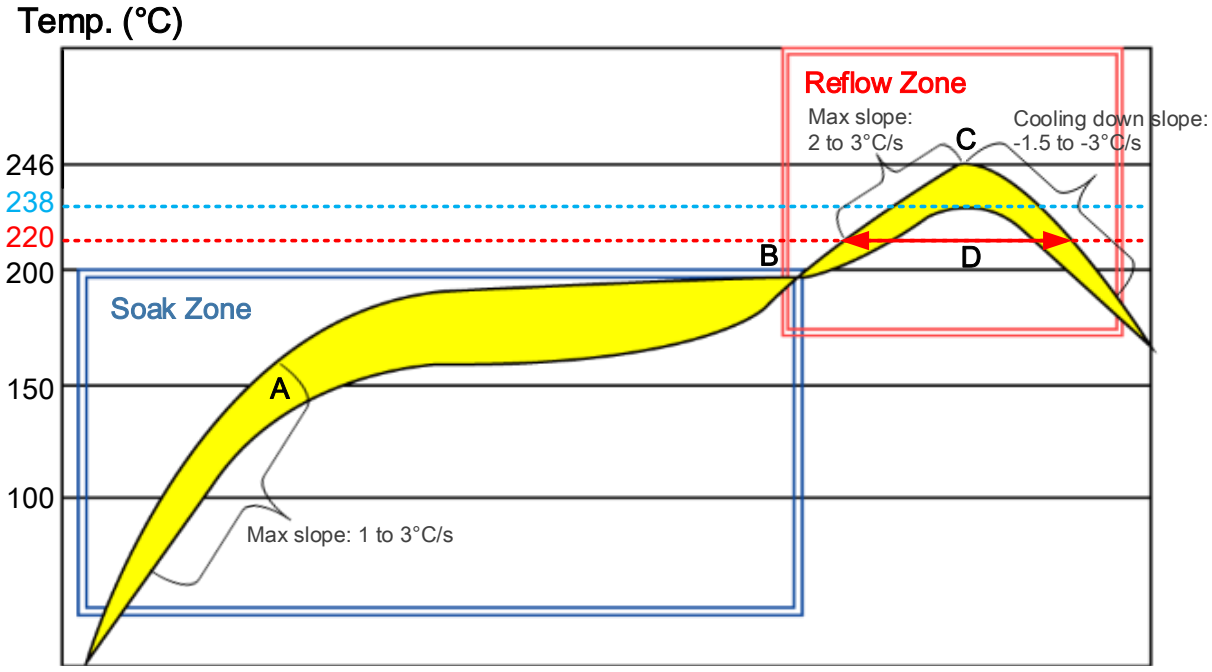

Figure 45: Recommended Reflow Soldering Thermal Profile

Table 33: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max. slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max. slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

7.3. Packaging

M65 QuecOpen is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

The following figures show the packaging details, measured in mm.

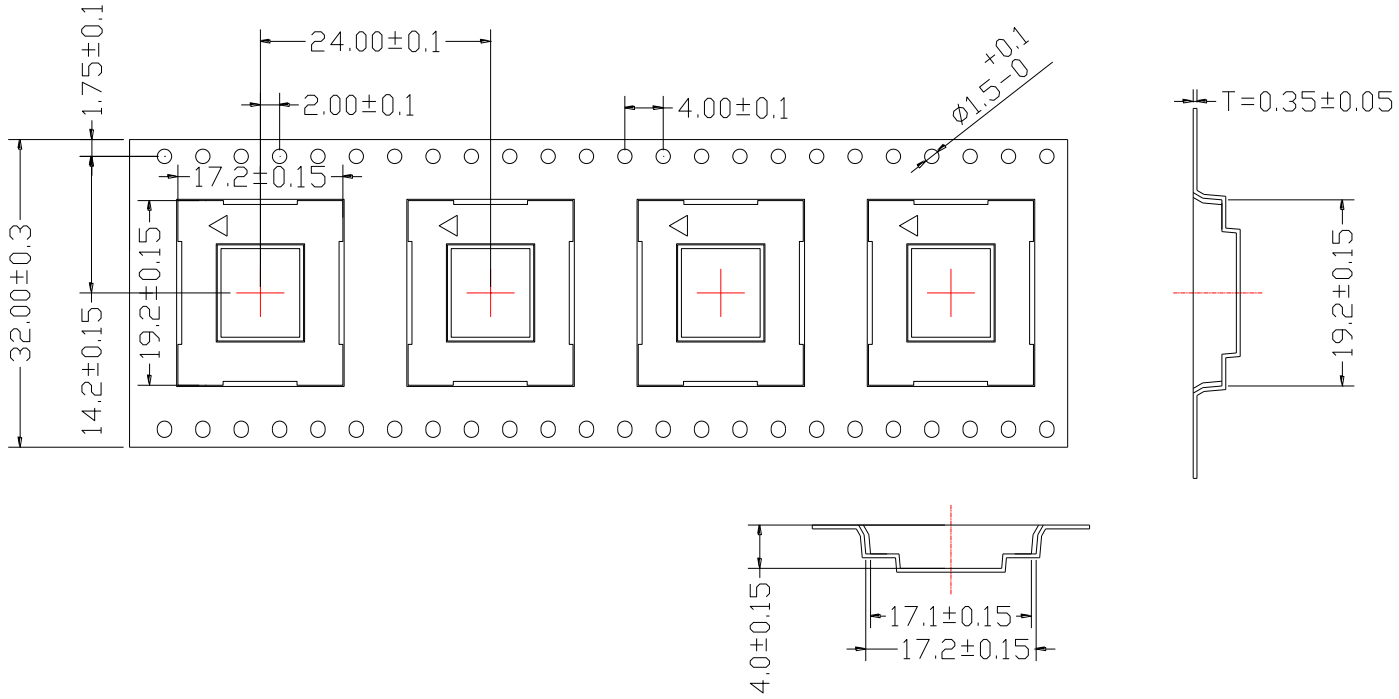

Figure 46: Tape Dimensions

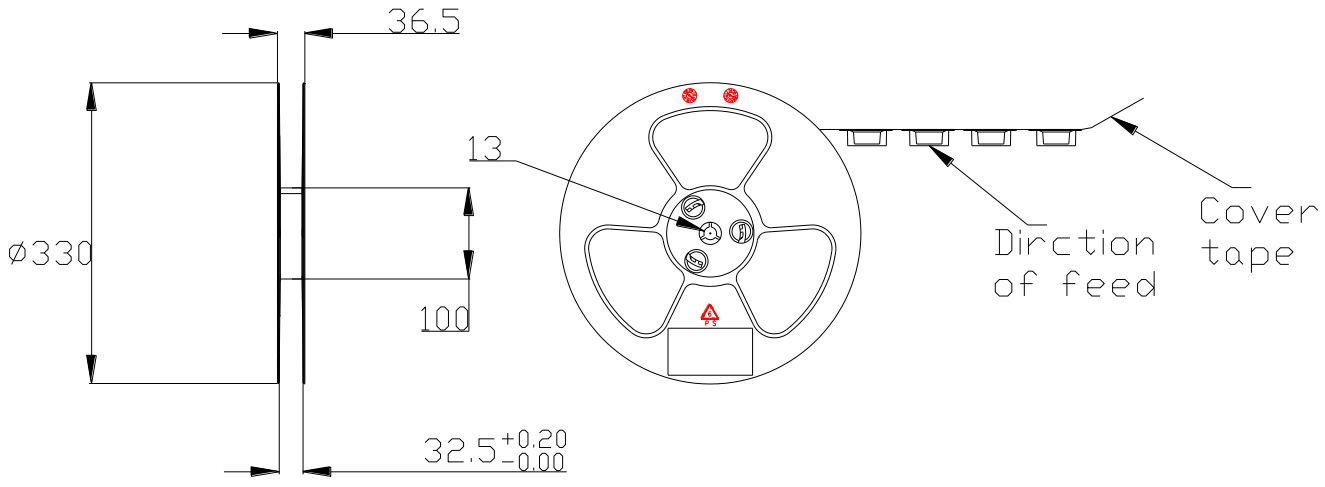

Figure 47: Reel Dimensions

Table 34: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 250 pcs	Minimum Package x 4=1000 pcs
M65 QuecOpen	250 pcs	Size: 370 mm × 350 mm × 56 mm N.W: 0.32 kg G.W: 1.08 kg	Size: 380 mm × 250 mm × 365 mm N.W: 1.28 kg G.W: 4.8 kg

8 Appendix References

Table 35: Related Documents

SN	Document Name	Description
[1]	Quectel_M65&M08-R_AT_Commands_Manual	M65 & M08-R QuecOpen AT commands manual
[2]	Quectel_GSM_UART_Application_Note	GSM UART interface application note
[3]	Quectel_GSM_EVB_User_Guide	GSM EVB user guide
[4]	ITU-T Draft new recommendation V.25ter	Serial asynchronous automatic dialing and control
[5]	Quectel_Module_Secondary_SMT_Application_Note	Module secondary SMT user guide
[6]	Quectel_GSM_Module_Digital_IO_Application_Note	GSM Module Digital IO Application Note
[7]	GSM 07.07	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[8]	GSM 07.10	Support GSM 07.10 multiplexing protocol
[9]	GSM 07.05	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[10]	GSM 11.14	Digital cellular telecommunications (Phase 2+); Specification of the (U)SIM Application Toolkit for the Subscriber Identity module – Mobile Equipment ((U)SIM – ME) interface
[11]	GSM 11.11	Digital cellular telecommunications (Phase 2+); Specification of the Subscriber Identity module – Mobile Equipment ((U)SIM – ME) interface

[12]	GSM 03.38	Digital cellular telecommunications (Phase 2+); Alphabets and language-specific information
[13]	GSM 11.10	Digital cellular telecommunications (Phase 2); Mobile Station (MS) conformance specification; Part 1: Conformance specification
[14]	Quectel_M65_QuecOpen_User_Guide	M65 QuecOpen user guide
[15]	Quectel_QuecOpen_Watchdog_Application_Note	QuecOpen watchdog application note

Table 36: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
ARFCH	Absolute Radio Frequency Channel Number
ASIC	Application Specific Integrated Circuit
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear to Send
DRX	Discontinuous Reception
DCD	Data Carrier Detection
DCE	Data Communications Equipment
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge

ESR	Equivalent Series Resistance
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
G.W	Gross Weight
HR	Half Rate
I/O	Input/Output
IC	Integrated Circuit
$I_O$max	Maximum Output Load Current
kbps	Kilo Bits Per Second
LED	Light Emitting Diode
ME	Mobile Equipment
MOQ	Minimum Order Quantity
MP	Manufacture Product
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
N.W	Net Weight
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCL	Power Control Level
PDU	Protocol Data Unit
PDP	Packet Data Protocol
PMOS	Positive Channel Metal Oxide Semiconductor
PPP	Point-to-Point Protocol

RF	Radio Frequency
RMS	Root Mean Square (value)
RTC	Real Time Clock
RX	Receive
(U)SIM	(Universal) Subscriber Identification Module
SGSN	Serving GPRS Support Node
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmission
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
$V_O$max	Maximum Output Voltage Value
$V_O$nom	Normal Output Voltage Value
$V_O$min	Minimum Output Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
$V_I$norm	Absolute Normal Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value

V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
Phonebook Abbreviations	
LD	(U)SIM Last Dialing phonebook (list of numbers most recently dialed)
MC	ME list of unanswered MT Calls (missed calls)
ON	(U)SIM (or ME) Own Numbers (MSISDNs) list
RC	ME list of Received Calls
SM	(U)SIM phonebook