M66-DS-OpenCPU

Hardware Design

GSM/GPRS Module Series

Rev. M66-DS-OpenCPU_Hardware_Design_V1.0

Date: 2016-09-26

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About the Document

History

Revision	Date	Author	Description
1.0	2016-09-26	King MA	Initial

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1 Introduction

This document defines the M66-DS-OpenCPU module, and describes its hardware interfaces which are connected with the customer application as well as its air interfaces.

This document can help customers quickly understand module interface specifications, as well as the electrical and mechanical details. Associated with application notes and user guide, customers can use the module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating M66-DS-OpenCPU module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobie while driving (even with a handsfree kit) causes distraction and can lead to an accident. You must comply with laws and regulations restrcting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers offers an Airplane Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals, clinics or other health care facilities. These requests are desinged to prevent possible interference with sensitive medical equipment.

	Cellular terminals or mobiles operating over radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

OpenCPU is an application solution where the module acts as the main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of OpenCPU solution. Especially, its advantage in reducing the product cost is greatly valued by customers. With the help of OpenCPU solution, development flow for wireless application and hardware design will be simplified. The main features of OpenCPU solution are as below:

1. Reduce the product development period.
2. Simplify the circuit design and reduce the cost.
3. Decrease the product's size.
4. Decrease the power consumption.
5. Upgraded via OpenCPU FOTA.
6. Improve the performance-to-price ratio and enhance the competitive strength.

M66-DS-OpenCPU module adopts the baseband processor with ARM7EJ-S™ core whose frequency can reach to 260MHz.

M66-DS-OpenCPU is a Quad-band GSM/GPRS engine that works at frequencies of GSM850MHz, EGSM900MHz, DCS1800MHz and PCS1900MHz. It features GPRS multi-slot class 12 and supports the GPRS coding schemes CS-1, CS-2, CS-3 and CS-4. For more details about GPRS multi-slot classes and coding schemes, please refer to ***Appendix B*** and ***Appendix C***.

M66-DS-OpenCPU is a SMD-type module with LCC package, and features an ultra-compact profile of 15.8mm × 17.7mm × 2.3mm. Furthermore, the module possesses abundant hardware interfaces and can be embedded into customer's applications conveniently.

Designed with power saving technique, the current consumption of M66-DS-OpenCPU is as low as 1.3mA in Sleep Mode when DRX is 5.

M66-DS-OpenCPU integrates internet service protocols such as TCP/UDP, HTTP, FTP, etc. Customers can use these internet service protocols easily by calling the API functions.

M66-DS-OpenCPU supports dual SIM dual standby function, which makes it the best choice for some applications.

M66-DS-OpenCPU supports Bluetooth interface which is fully compliant with Bluetooth specification 3.0.

The module fully complies with the RoHS directive of the European Union.

2.2. Key Features

The following table describes the detailed features of M66-DS-OpenCPU.

Table 1: Key Features

Feature	Implementation
Power Supply	Single supply voltage: 3.3V ~ 4.6V Typical supply voltage: 4V
Power Saving	Typical power consumption in SLEEP mode: 1.3 mA @DRX=5 1.2 mA @DRX=9
Frequency Bands	● Quad-band: GSM850, EGSM900, DCS1800, PCS1900 ● The module can search these frequency bands automatically ● The frequency bands can be set by **AT+QBAND** command ● Compliant to GSM Phase 2/2+
GSM Class	Small MS
Transmitting Power	● Class 4 (2W) at GSM850 and EGSM900 ● Class 1 (1W) at DCS1800 and PCS1900
GPRS Connectivity	● GPRS multi-slot class 12 (default) ● GPRS multi-slot class 1~12 (configurable) ● GPRS mobile station class B
DATA GPRS	● GPRS data downlink transfer: max. 85.6kbps ● GPRS data uplink transfer: max. 85.6kbps ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Support the PAP (Password Authentication Protocol) usually used for PPP connections ● Internet service protocols TCP/UDP, FTP, HTTP, NTP, PING ● Support Packet Broadcast Control Channel (PBCCH) ● Support Unstructured Supplementary Service Data (USSD)
Temperature Range	● Operation temperature range: -35°C ~ +75°C [1)] ● Extended temperature range: -40°C ~ +85°C [2)]
Bluetooth	● Support Bluetooth specification 3.0 ● Output Power: Class 1 (Typical 7.5dBm)
SMS	● Text and PDU mode ● SMS storage: SIM card

SIM Interface	● Support SIM card: 1.8V, 3.0V ● Support dual SIM dual standby
SD Interface	● Only support 1bit serial mode ● The data rate up to 48MHz in serial mode
Audio Features	Speech codec modes: ● Half Rate (ETS 06.20) ● Full Rate (ETS 06.10) ● Enhanced Full Rate (ETS 06.50/06.60/06.80) ● Adaptive Multi-Rate (AMR) ● Echo Suppression ● Noise Reduction ● Embedded one amplifier of class AB with maximum driving power up to 870mW
UART Interfaces	**UART Port:** ● Seven lines on UART port interface ● Used for AT command communication, GPRS data transmission, etc. ● Multiplexing function ● Support autobauding from 4800bps to 115200bps **Debug Port:** ● Two lines on debug port interface DBG_TXD and DBG_RXD ● Debug Port only used for firmware debugging **Auxiliary Port:** ● Used for AT command communication
Phonebook Management	Support phonebook types: SM, ME, ON, MC, RC, DC, LD, LA
SIM Application Toolkit	Support SAT class 3, GSM 11.14 Release 99
Real Time Clock	Supported
Physical Characteristics	Size: 15.8±0.15 × 17.7±0.15 × 2.3±0.2mm Weight: Approx. 1.3g
Firmware Upgrade	● Via UART Port ● Via OpenCPU FOTA
Antenna Interface	Connected to antenna pad with 50 Ohm impedance control

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP compliant again.

Table 2: Coding Schemes and Maximum Net Data Rates over Air Interface

Coding Scheme	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	9.05kbps	18.1kbps	36.2kbps
CS-2	13.4kbps	26.8kbps	53.6kbps
CS-3	15.6kbps	31.2kbps	62.4kbps
CS-4	21.4kbps	42.8kbps	85.6kbps

2.3. Functional Diagram

The following figure shows a block diagram of M66-DS-OpenCPU and illustrates the major functional parts.

- Memory
- Radio frequency part
- Power management
- The peripheral interface
  - Power supply
  - Turn-on/off interface
  - UART interface
  - Audio interface
  - PCM interface
  - SPI interface
  - SD interface
  - I2C interface
  - SIM interface
  - ADC interface
  - RF interface
  - BT interface

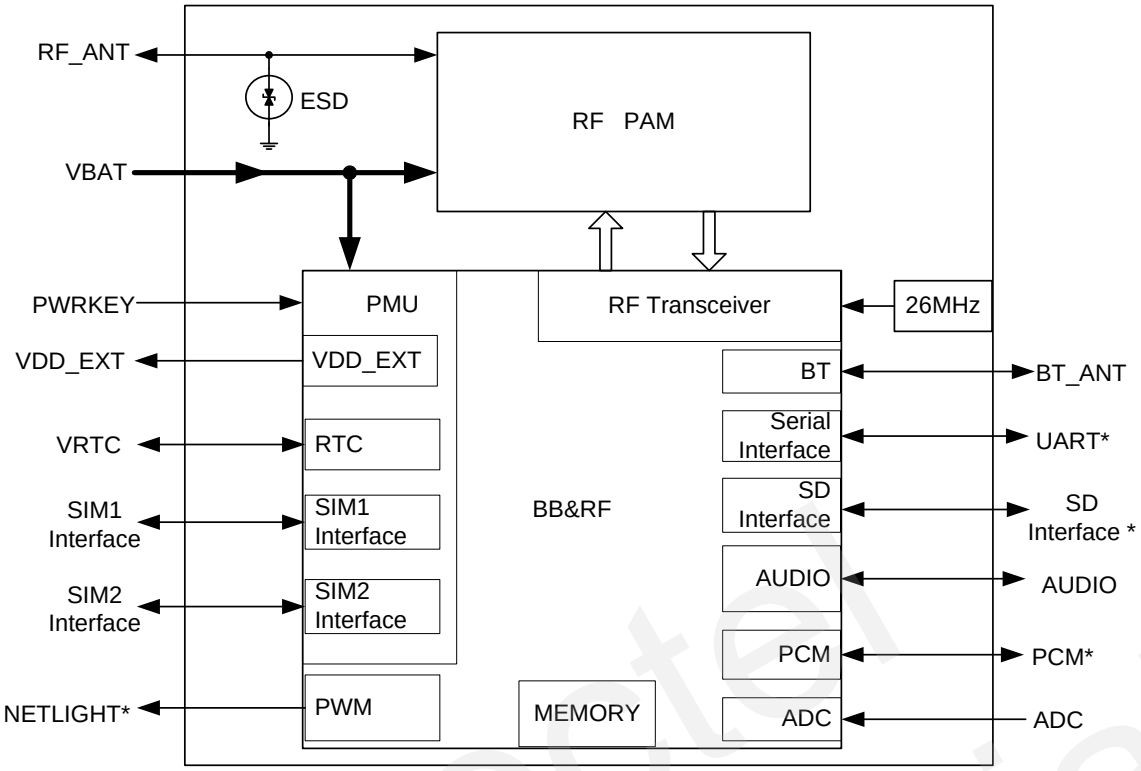

Figure 1: Module Functional Diagram

NOTE

About alternate functions of the interfaces marked with "*", please refer to ***Table 5***.

2.4. Pin Assignment

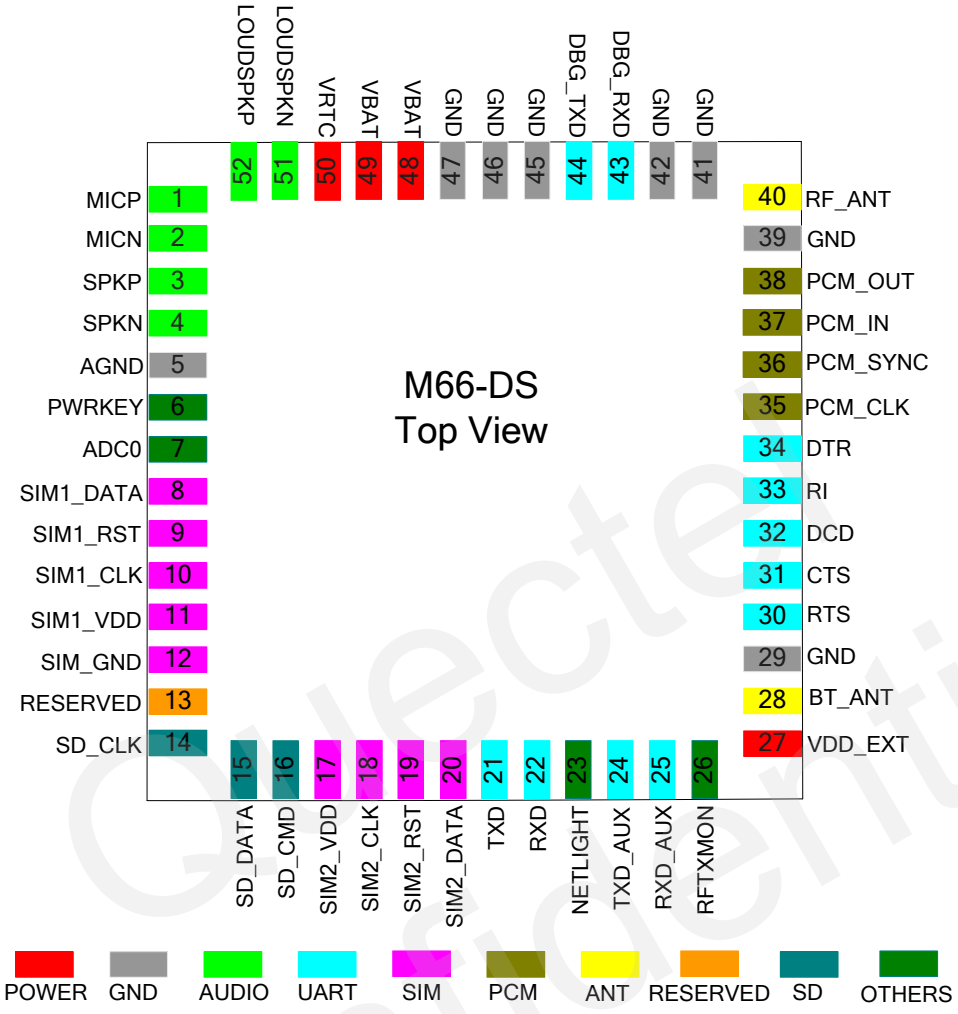

Figure 2: Pin Assignment

NOTE

Keep all reserved pins open.

Table 3: I/O Parameters Definition

Type	Description
IO	Bidirectional input/output
DI	Digital input

DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output

Table 4: Pin Description

Power Supply					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	48, 49	PI	Main power supply of module: VBAT=3.3V~4.6V	$V_I$max=4.6V $V_I$min=3.3V $V_I$norm=4.0V	It must be able to provide sufficient current up to 1.6A in a burst transmission.
VRTC	50	IO	Power supply for RTC when VBAT is not available for powering the system. Charging for backup battery or golden capacitor when the VBAT is applied.	$V_I$max=3.3V $V_I$min=1.5V $V_I$norm=2.8V $V_O$max=3V $V_O$min=2V $V_O$norm=2.8V $I_O$max=2mA Iin≈10uA	If unused, keep this pin open.
VDD_EXT	27	PO	Supply 2.8V voltage for external circuit	$V_O$max=2.9V $V_O$min=2.7V $V_O$norm=2.8V $I_O$max=20mA	1. If unused, keep this pin open. 2. Recommend adding a 2.2~4.7uF bypass capacitor, when using this pin for power supply.
GND	29, 39, 41, 42, 45, 46, 47		Ground		
Turn on/off					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

PWRKEY	6	DI	Power on/off key. PWRKEY should be pulled down for a moment to turn on or turn off the system.	V_{IL}max= 0.1×VBAT V_{IH}min= 0.6×VBAT V_{IH}max=3.1V	
Audio Interface					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MICP MICN	1, 2	AI	Positive and negative voice input	Refer to ***Chapter 3.7***	If unused, keep these pins open.
SPKP SPKN	3, 4	AO	Channel 1 positive and negative voice output		If unused, keep these pins open. Support both voice and ringtone output.
AGND	5		Analog ground. Separate ground connection for external audio circuits.		If unused, keep this pin open.
LOUDSPKP LOUDSPKN	52 51	AO	Channel 2 positive and negative voice output		1. If unused, keep these pins open. 2. Integrate a Class- AB amplifier internally. 3. Support both voice and ringtone output.
Network Status Indicator					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NETLIGHT	23	DO	Network status indication	V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	If unused, keep this pin open.
UART Port					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TXD	21	DO	Transmit data	V_{IL}min=0V V_{IL}max= 0.25×VDD_EXT V_{IH}min= 0.75×VDD_EXT	If only use TXD, RXD and GND to communicate, recommend keeping all other pins open.
RXD	22	DI	Receive data		
DTR	34	DI	Data terminal ready		

RI	33	DO	Ring indication	V_{IH}max= VDD_EXT+0.2 V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	
DCD	32	DO	Data carrier detection		
CTS	31	DO	Clear to send		
RTS	30	DI	Request to send		
Debug Port					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_ TXD	44	DO	Transmit data	The same as above	If unused, keep these pins open.
DBG_ RXD	43	DI	Receive data		
Auxiliary Port					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TXD_ AUX	24	DO	Transmit data	The same as above	If unused, keep these pins open.
RXD_ AUX	25	DI	Receive data		
SIM Interface					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SIM1_ VDD SIM2_ VDD	11 17	PO	Power supply for SIM card	The voltage can be selected by software automatically. Either 1.8V or 3.0V.	All signals of SIM interface should be protected against ESD with a TVS diode array. Maximum trace length is 200mm from the module pad to SIM card holder.
SIM1_ CLK SIM2_ CLK	10 18	DO	SIM clock	V_{OL}max= 0.15×SIM_VDD V_{OH}min= 0.85×SIM_VDD	
SIM1_ DATA SIM2_ DATA	8 20	IO	SIM data	V_{IL}max= 0.25×SIM_VDD V_{IH}min= 0.75×SIM_VDD V_{OL}max= 0.15×SIM_VDD V_{OH}min= 0.85×SIM_VDD	

SIM1_ RST SIM2_ RST	9 19	DO	SIM reset	V_{OL}max= 0.15×SIM_VDD V_{OH}min= 0.85×SIM_VDD	
SIM1_ PRESENCE	34	I	SIM1 card detection	V_{IL}min =0V V_{IL}max = 0.25×VDD_EXT V_{IH}min = 0.75×VDD_EXT V_{IH}max = VDD_EXT+0.2	Default DTR function. Not supported by software presently.
SIM_ GND	12		SIM ground		
ADC					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	7	AI	General purpose analog to digital converter	Voltage range: 0V to 2.8V	If unused, keep this pin open.
PCM					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_ CLK	35	DO	PCM clock	V_{IL}min= 0V V_{IL}max= 0.25×VDD_EXT V_{IH}min= 0.75×VDD_EXT V_{IH}max= VDD_EXT+0.2 V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	If unused, keep these pins open.
PCM_ SYNC	36	DO	PCM frame synchronization		
PCM_IN	37	DI	PCM data input		
PCM_ OUT	38	DO	PCM data output		
SD Card					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CMD	16	DO	SD command	V_{IL}min=0V V_{IL}max= 0.25×VDD_EXT V_{IH}min= 0.75×VDD_EXT V_{IH}max=	If unused, keep these pins open.
SD_CLK	14	DO	SD clock		
SD_ DATA	15	I/O	SD data		

				VDD_EXT+0.2 V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	
Antenna Interface					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RF_ANT	40	IO	GSM antenna pad	Impedance of 50Ω	
BT_ANT	28	IO	BT antenna pad	Impedance of 50Ω	If unused, keep this pin open.
Transmitting Signal Indication					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RFTXMON	26	DO	Transmission signal indication	V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	If unused, keep this pin open.
Other Interface					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	13				Keep this pin open.

Table 5: Multiplexed Functions

PIN Name	PIN No.	Mode1 (Default)	Mode 2	Mode 3	Mode 4
NETLIGHT	23	NETLIGHT	GPIO	PWM	
DTR	34	DTR	GPIO	EINT	SIM1_PRESENCE
RI	33	RI	GPIO	I2C_SCL	
DCD	32	DCD	GPIO	I2C_SDA	
CTS	31	CTS	GPIO		
RTS	30	RTS	GPIO		
RXD_AUX	25	RXD_AUX	GPIO		

TXD_AUX	24	TXD_AUX	GPIO	
PCM_CLK	35	PCM_CLK	GPIO	SPI_CS
PCM_ SYNC	36	PCM_SYNC	GPIO	SPI_MISO
PCM_IN	37	PCM_IN	GPIO	SPI_CLK
PCM_OUT	38	PCM_OUT	GPIO	SPI_MOSI

2.5. Operating Modes

The table below briefly summarizes the various operating modes.

Table 6: Overview of Operating Modes

Mode	Function	
Normal Operation	GSM/GPRS Sleep	After enabling sleep mode by calling **Ql_SleepEnable()**, the module will automatically enter into Sleep Mode when CPU is in idle state. In this case, the current consumption of module will reduce to the minimal level. During Sleep Mode, the module can still receive paging message and SMS from the network normally.
	GSM IDLE	Software is active. The module has registered on GSM network, and it is ready to send and receive GSM data.
	GSM TALK	GSM connection is ongoing. In this mode, the power consumption is decided by the configuration of Power Control Level (PCL), dynamic DTX control and the working RF band.
	GPRS IDLE	The module is not registered on GPRS network, and it is not reachable through GPRS channel.
	GPRS STANDBY	The module is registered on GPRS network, but no GPRS PDP context is active. The SGSN knows the Routing Area where the module is located at.
	GPRS READY	The PDP context is active, but no data transfer is ongoing. The module is ready to receive or send GPRS data. The SGSN knows the cell where the module is located at.
	GPRS DATA	There is GPRS data in transfer. In this mode, power consumption is decided by the PCL, working RF band and GPRS multi-slot configuration.

POWER DOWN	Normal shutdown calling **Ql_PowerDown()** or using the PWRKEY pin. The power management ASIC disconnects the power supply from the base band part of the module, and only the power supply for the RTC is remained. Software is not active. The UART interfaces are not accessible. Operating voltage (connected to VBAT) remains applied.
Minimum Functionality Mode (without removing power supply)	**AT+CFUN** command can set the module to the minimum functionality mode without removing the power supply. In this case, the RF part of the module will not work or the SIM card will not be accessible, or both RF part and SIM card will be disabled; but the UART port is still accessible. The power consumption in this case is very low.

2.6. Flash Memory Allocation

A 32M-bit flash memory is used in the module. The flash memory allocation is shown as below.

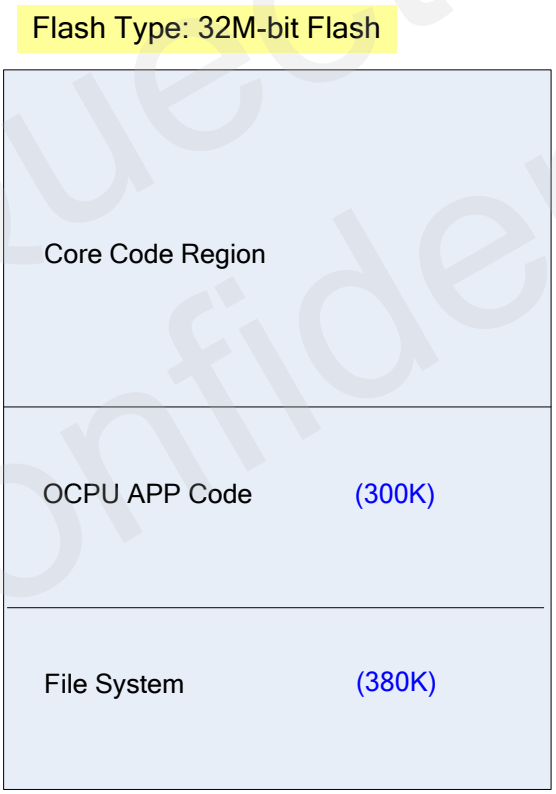

Figure 3: FLASH Memory Allocation

M66-DS-OpenCPU module allocates 300KB space for customer's code and 380KB file system space which is used to store the data (e.g. system configuration file, temporary data, image, multimedia file, and so on) related to file operation.

- RAM

M66-DS-OpenCPU reserves 100KB RAM space for the embedded application and provides about 500KB dynamic memory at most.

3 Application Interfaces

3.1. General Description

The module adopts LCC package and has 52 pins. The following chapters provide detailed descriptions about these pins.

- Power supply
- Power on/down
- Power saving
- RTC
- Serial interfaces
- Audio interfaces
- SIM card interface
- SD card interface
- PCM interface
- SPI and I2C interface
- ADC
- External interrupts
- PWM
- GPIO
- RF transmitting signal indication

3.2. Power Supply

3.2.1. Power Features of the Module

The power supply is important during GSM terminals design. Due to the 577us radio burst in GSM every 4.615ms, the power supply must be able to deliver high current peaks in a burst period. During these peaks, drops on the supply voltage must not exceed minimum working voltage of the module.

For the M66-DS-OpenCPU module, the maximum current consumption could reach 1.6A during a burst transmission. It will cause a large voltage drop on the VBAT. In order to ensure stable operation of the module, it is recommended that the maximum voltage drop for VBAT during burst transmission does not exceed 400mV.

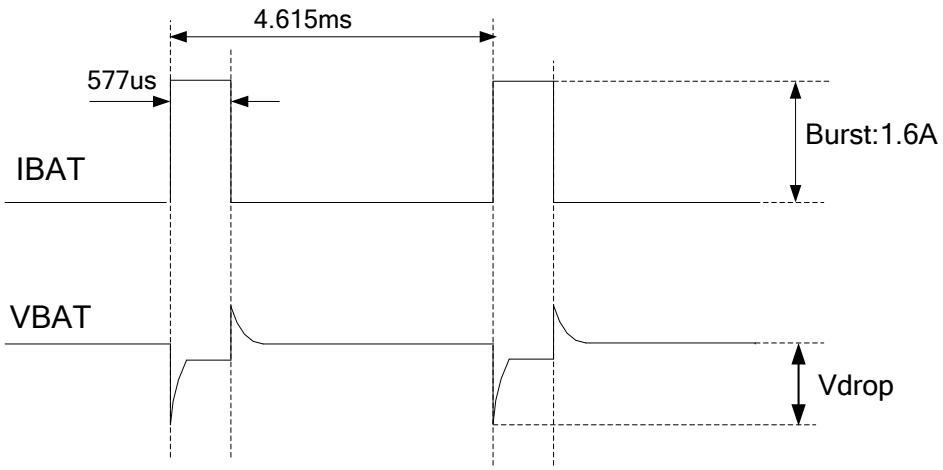

Figure 4: Voltage Ripple during Transmitting

3.2.2. Decrease Supply Voltage Drop

The power supply range of the module is from 3.3V to 4.6V. Make sure that the input voltage will never drop below 3.3V even during a burst transmission. If the power voltage drops below 3.3V, the module will be turned off automatically. For better power performance, it is recommended to place a 100uF tantalum capacitor with low ESR (ESR=0.7Ω) and a ceramic capacitor (100nF~1uF) near the VBAT pin. In order to improve the RF interference, other low capacitance capacitors should be placed close to the VBAT pin. A reference circuit is illustrated in the following figure.

The VBAT trace should be wide enough to ensure that there is not too much voltage drop occurring during burst transmission. The width of trace should be no less than 2mm; and in principle, the longer the VBAT trace, the wider it will be.

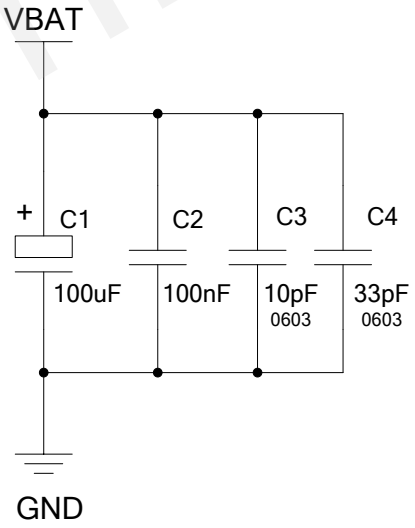

Figure 5: Reference Circuit for the VBAT Input

3.2.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of module largely depends on the power source. The power supply is capable of providing sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested to use an LDO as the module's power supply. If there is a big voltage difference between the input source and the desired output (VBAT), a switcher power converter is recommended to be used as the power supply.

The following figure shows a reference design for +5V input power source. The designed output for the power supply is 4.0V and the maximum load current is 3A. In addition, in order to get a stable output voltage, a zener diode is placed close to the pins of VBAT. As to the zener diode, it is suggested to use a zener diode whose reverse zener voltage is 5.1V and dissipation power is more than 1 Watt.

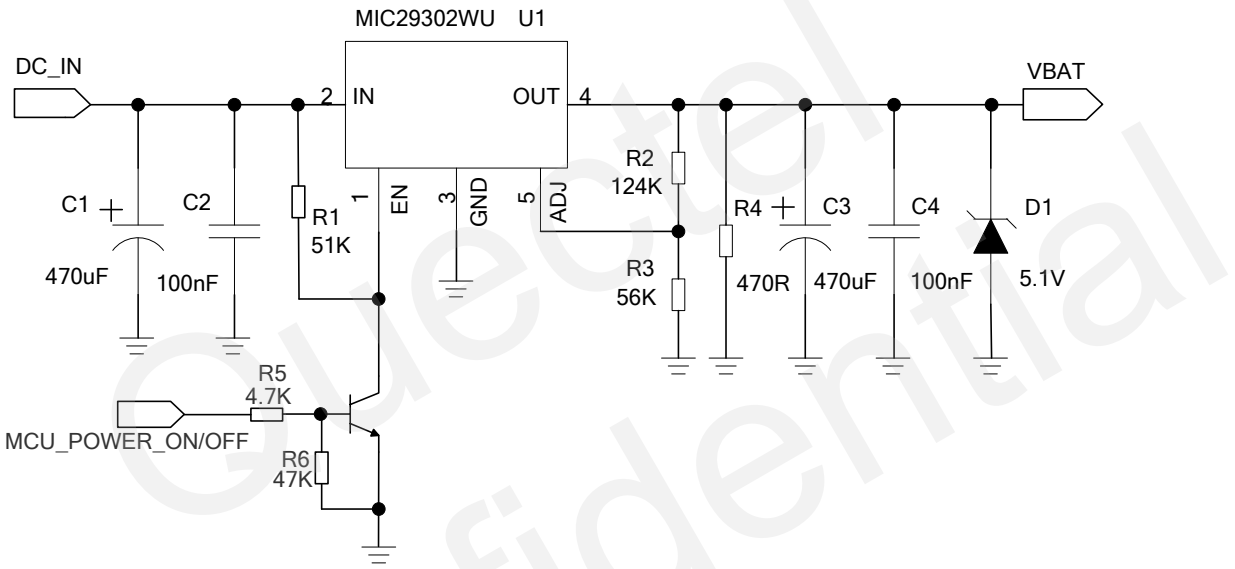

Figure 6: Reference Circuit for Power Supply

NOTE

It is suggested to control the module's main power supply (VBAT) via LDO enable pin to restart the module when the module has become abnormal. Power switch circuit like P-channel MOSFET switch circuit can also be used to control VBAT.

3.2.4. Monitor Power Supply

The module can monitor the supply voltage by using **AT+CBC** command or calling **RIL_GetPowerSupply()**. Your application program can start a timer and periodically use **AT+CBC** command or call **RIL_GetPowerSupply()** to check the power supply.

For more information about the software design, please refer to the ***document [12]***.

3.3. Power on and down Scenarios

3.3.1. Power on

The module can be turned on by driving PWRKEY pin to a low level voltage. An open collector driver circuit is recommended to be used to control the PWRKEY. A simple reference circuit is illustrated as below.

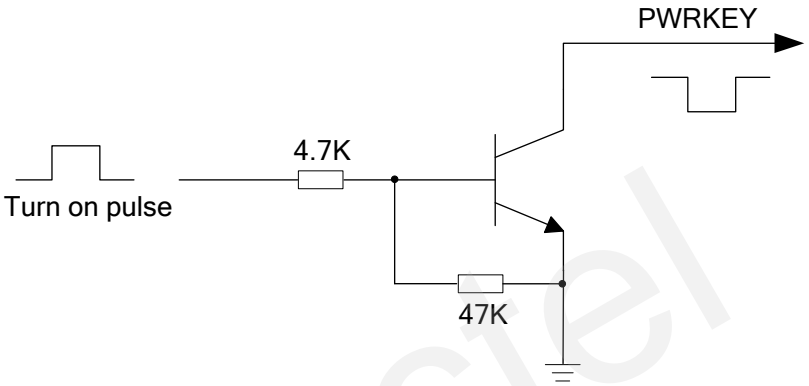

Figure 7: Turn on the Module with an Open-collector Driver

The other way to control the PWRKEY is through a button directly. While pressing the key, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown below.

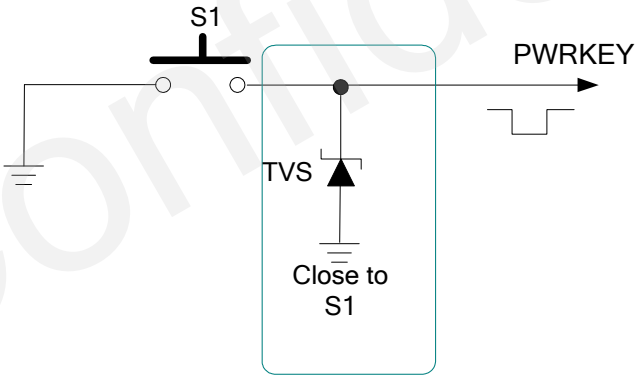

Figure 8: Turn on the Module with a Button

The turn-on timing is illustrated below.

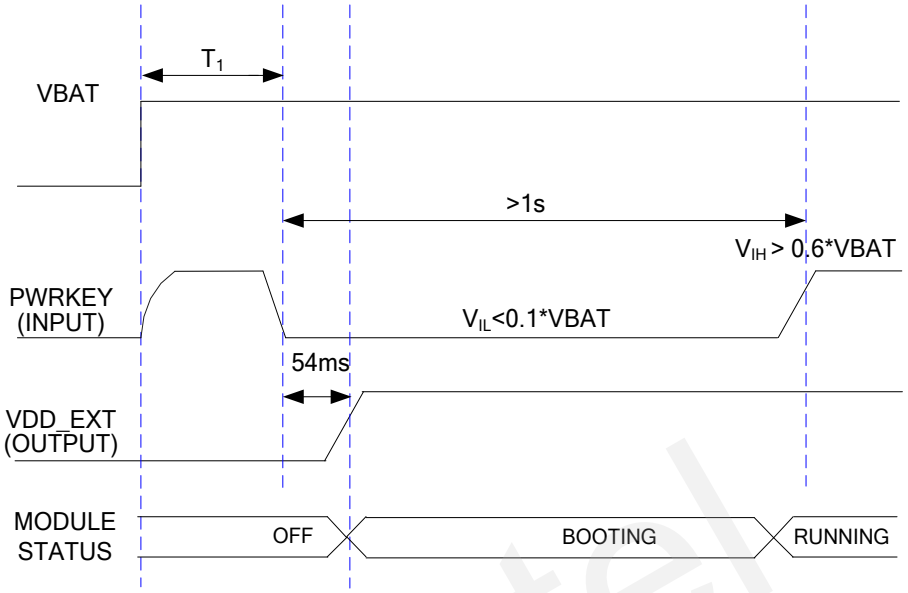

Figure 9: Turn-on Timing

NOTES

1. Make sure that VBAT voltage is stable before pulling down PWRKEY pin. The time of T_1 is recommended to be 100ms.
2. Set PWRKEY low for at least 1 second to turn on the system. If the PWRKEY is set as low continuously, the module can also be turned on, but in this case, PWRKEY cannot be used to turn off the module.

3.3.2. Power down

The following methods can be used to turn off the module.

- Normal power down procedure: Turn off module using the PWRKEY pin
- Normal power down procedure: Turn off module by executing **AT+QPOWD** command or calling API **QI_PowerDown()**
- Under-voltage automatic shutdown: Take effect when under-voltage is detected.

3.3.2.1. Power down Module Using the PWRKEY Pin

Set the PWRKEY pin low for a certain time and then the module will be turned off. During turn-off, the module will log off from the network and save important data. As the time needed for logging off from network is related to the local mobile network, it is recommended to delay for about 12 seconds before

disconnecting the power supply or restarting the module.

After the PWRKEY pin is set to low, the module will be powered down by calling API function. For more information about software design, please refer to *the* ***document [12]***.

After turn-off, the module enters into POWER DOWN Mode. The turn-off timing is shown as below.

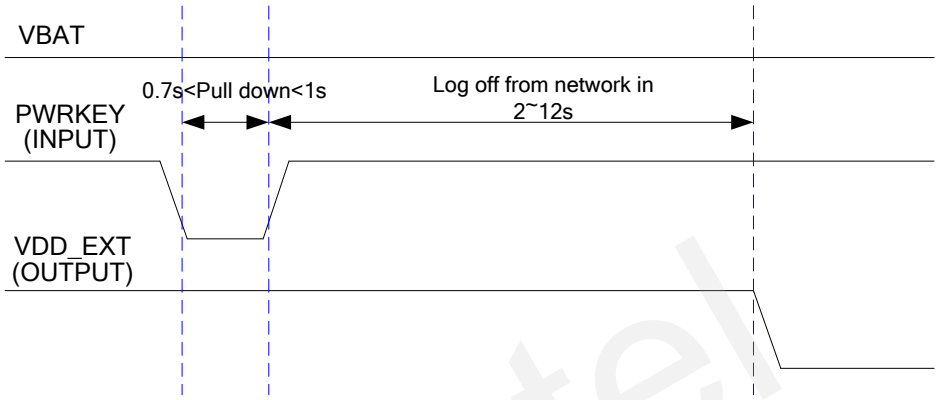

Figure 10: Turn-off Timing

NOTE

If the PWRKEY pin is used to turn off the module, it cannot be set to low continuously. Otherwise, the module will restart after being turned off.

3.3.2.2. Power down Module Using the API Function

The module can achieve normal turn-off through calling an API function **Ql_PowerDown()**.

For detailed information about the software design, please refer to the ***document [12]***.

3.3.2.3. Under-voltage Automatic Shutdown

Under-voltage will cause the module to turn off. The module will constantly monitor the voltage applied on the VBAT. If any circumstance shown below occurs, the module will notify customer's application through Callback functions.

- VBAT voltage is ≤ 3.5V: under-voltage warning.
- VBAT voltage is <3.3V: under-voltage turn-off.

For detailed information about the software design, please refer to the ***document [12]***.

3.3.3. Recommended Turn-on Structure for OpenCPU System

In order to ensure the stability of OpenCPU system, it is suggested to use a low-power MCU to monitor the module status. The MCU should possess several GPIOs and one ADC interface. The system structure is shown in the figure below. This structure possesses two advantages:

- When the VBAT voltage detected by ADC is too low, the MCU will turn off the module by controlling PWRKEY pin and switch off power supply by controlling the PMOS transistor.
- Normally, the module outputs periodic pulse to the MCU. If the MCU does not detect the pulse within the stipulated time, the MCU will switch off VBAT and then turn on the module again.

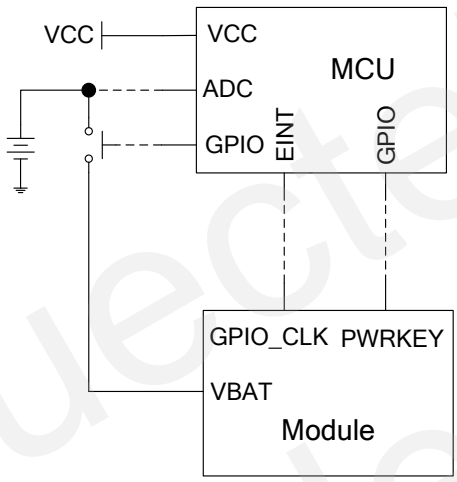

Figure 11: Recommended Turn-on Structure for OpenCPU System

Furthermore, a watchdog component can be used to control the power of module. A watchdog component with minimum timeout of 1.6s should be used, for instance, TI's TPS3823-33DBVR. One GPIO of the module should be connected to the WDI pin of the watchdog and change the electrical level of the WDI pin timely. If timeout occurs, the watchdog will switch off the power of the module. The sketch map for watchdog is shown as below.

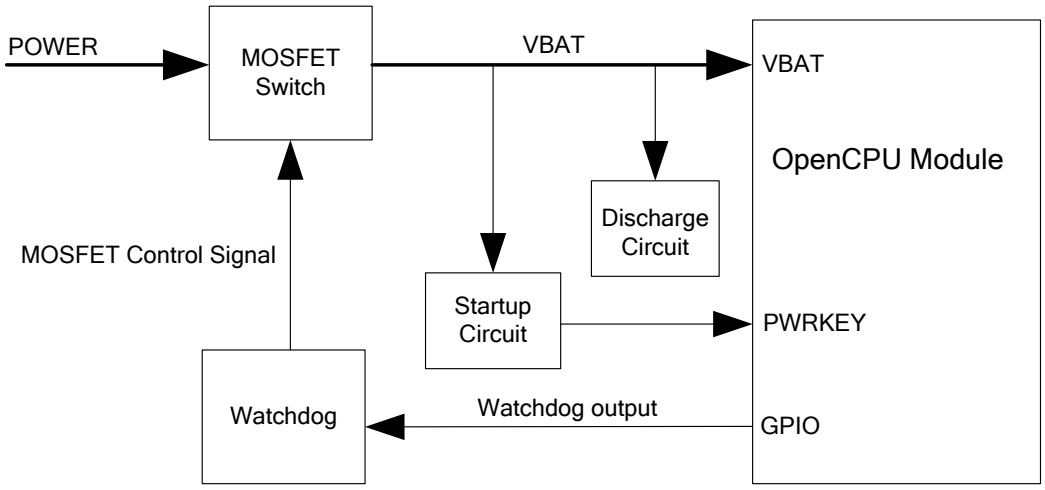

Figure 12: Sketch Map for Watchdog

NOTE

If the power of the module is controlled by watchdog circuit and the module is only powered by VRTC, the real time will have an error of about 5 minutes a day when the power is switched off.

3.4. Power Saving

Based on system requirements, there are two methods to drive the module to enter into low current consumption status. One is to use the AT command to make the module enter into Minimum Functionality Mode, and the other is to use the API function to make the module enter into Sleep Mode.

3.4.1. Minimum Functionality Mode

M66-DS-OpenCPU module reduces its functionality to a minimum level in order to minimize the current consumption in Minimum Functionality Mode. The module can enter into Minimum Functionality Mode through using **AT+CFUN=0** command. When using **AT+CFUN?** command for querying the module's current functionality status and the returned value is not equal to 1, the module can enter into Full Functionality Mode through using **AT+CFUN=1** command. For detailed information about the software design, please refer to the ***document [12]***.

3.4.2. Sleep Mode

After entering into Sleep Mode, M66-DS-OpenCPU module can still receive calls, SMS and GPRS data, but the serial interfaces do not work. The Sleep Mode is disabled by default. The module can enter into Sleep Mode when it is idle through calling the API function **Ql_SleepEnable()**.

When M66-DS-OpenCPU module is in Sleep Mode, the following methods can wake it up.

- Incoming call
- SMS or MMS
- GPRS data
- External interrupts
- System timer timeout

The following methods can make the module exit from Sleep Mode.

- Call the API function **Ql_SleepDisable()** when the application program is executed.

For detailed information about the software design, please refer to the ***document [12]***.

3.5. RTC

The RTC (Real Time Clock) function is supported. The RTC is designed to work with an internal power supply.

There are three kinds of designs for RTC backup power:

- **Use VBAT as the RTC power source**

When the module is turned off and the main power supply (VBAT) is remained, the real time clock is still active as the RTC core is powered by VBAT. In this case, the VRTC pin can be kept floating.

- **Use VRTC as the RTC power source**

If the main power supply (VBAT) is removed after the module is turned off, a backup power such as a coin-cell battery (rechargeable or non-chargeable) or a supercapacitor can be used to power the VRTC pin to keep the real time clock active.

- **Use VBAT and VRTC as the RTC power source**

As only power the VRTC pin to keep the RTC active will lead an error of about 5 minutes a day, it is recommended to power VBAT and VRTC pin at the same time when RTC function is needed. The

recommended supply for RTC core circuits are shown as below.

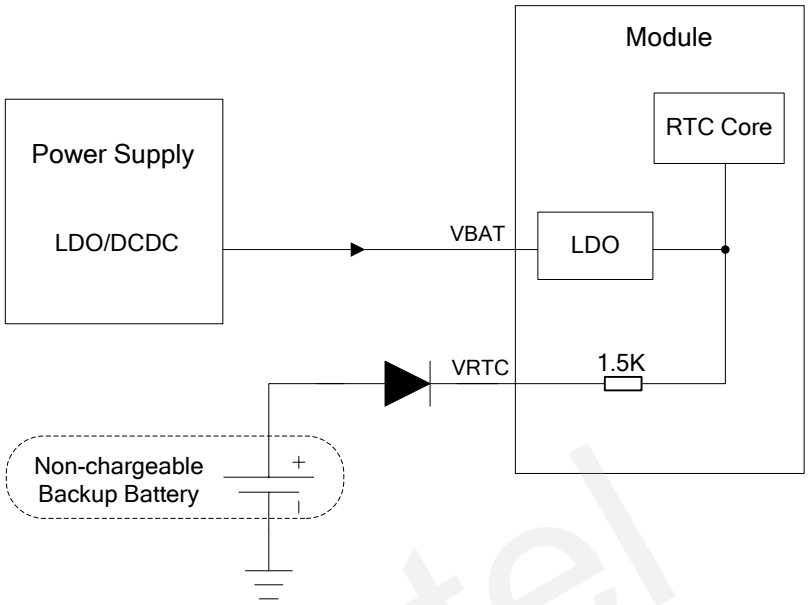

Figure 13: VRTC is Powered by a Non-chargeable Battery

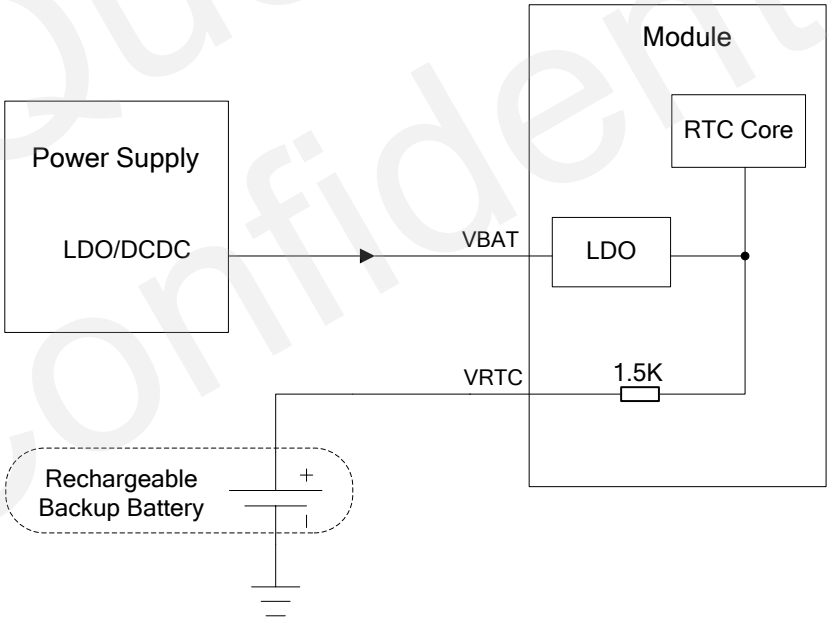

Figure 14: VRTC is Powered by a Rechargeable Battery

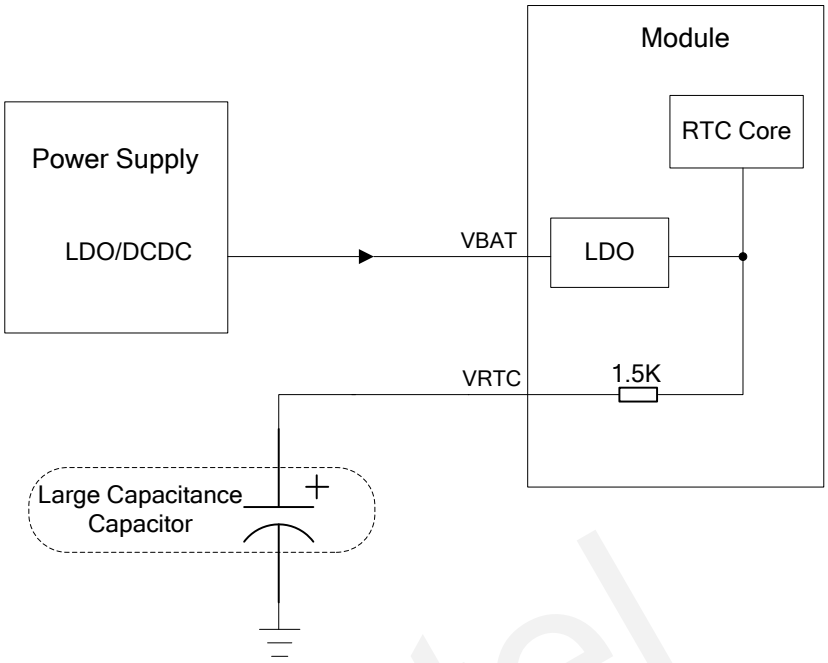

Figure 15: VRTC is Powered by a Capacitor

A rechargeable or non-chargeable coin-cell battery can also be used here. For more information, please visit http://www.sii.co.jp/en/.

API functions relating to RTC are shown as below:

- Get RTC time: **Ql_GetLocalTime()**
- Set RTC time: **Ql_SetLocalTime()**

For detailed information about the software design, please refer to the ***document [12].***

NOTE

If you want to keep an accurate real time, please keep the main power supply VBAT alive .

3.6. Serial Interfaces

M66-DS OpenCPU module provides three serial ports: UART Port, Debug Port and Auxiliary UART Port. It is designed DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection. The module adopts fixed baudrate and its default baudrate is 115200bps. It supports autobauding from 4800bps to 115200bps.

The UART Port:

- TXD: Send data to RXD of DTE.
- RXD: Receive data from TXD of DTE.
- RTS: Request to send.
- CTS: Clear to send.
- DTR: DTE is ready and inform DCE (this pin can wake up the module).
- RI: Ring indicator (when there is a call, SMS or URC output, the module will inform DTE with the RI pin.)
- DCD: Data carrier detection.

The Debug Port:

- DBG_TXD: Send data to the RXD of DTE
- DBG_RXD: Receive data from the TXD of DTE

The Auxiliary UART Port:

- TXD_AUX: Send data to the RXD of DTE
- RXD_AUX: Receive data from the TXD of DTE

The logic levels of these serial interfaces are described in the following table.

Table 7: Logic Levels of UART Interfaces

Parameter	Min.	Max.	Unit
V_{IL}	0	0.25×VDD_EXT	V
V_{IH}	0.75×VDD_EXT	VDD_EXT +0.2	V
V_{OL}	0	0.15×VDD_EXT	V
V_{OH}	0.85×VDD_EXT	VDD_EXT	V

Table 8: Pin Definition of UART Interfaces

Interface	Pin Name	Pin No.	Description
UART Port	TXD	21	Transmit data
	RXD	22	Receive data

	DTR	34	Data terminal ready
	RI	33	Ring indicator
	DCD	32	Data carrier detection
	CTS	31	Clear to send
	RTS	30	Request to send
Debug Port	DBG_RXD	43	Receive data
	DBG_TXD	44	Transmit data
Auxiliary UART Port	RXD_AUX	25	Receive data
	TXD_AUX	24	Transmit data

NOTE

If DCD, RI, DTR, CTS and RTS are not used, they can be multiplexed as GPIOs. For more details, please refer to ***Chapter 3.15***.

Functions and events relating to serial interfaces are as below:

- **Ql_UART_Register**: register a callback for the specified serial port.
- **Ql_UART_Open**: open the specified serial port.
- **Ql_UART_Write**: send data to the specified serial port.
- **Ql_UART_Read**: read data from the specified serial port.
- **Ql_UART_SetDCBConfig**: set DCB of serial port.
- **EVENT_UART_READY_TO_READ**: read indication when data comes.

For detailed information about the software design, please refer to the ***document [12].***

3.6.1. UART Port

3.6.1.1. Features of UART Port.

- 8 data bits, no parity bit, one stop bit.
- Firmware upgrade and data communication.
- Supported baud rates are as below:
  300, 600, 2400, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800bps.
- The module adopts a fixed baud rate and its default baud rate is 115200bps.
- Support hardware flow control, but it is disabled by default.

NOTES

1. The API function **QI_UART_SetDCBConfig** can be used to set different baudrate.
2. The API function **QI_UART_Open** can be used to set hardware flow control.

3.6.1.2. Reference Design for UART Port

A reference design for UART Port is shown as below.

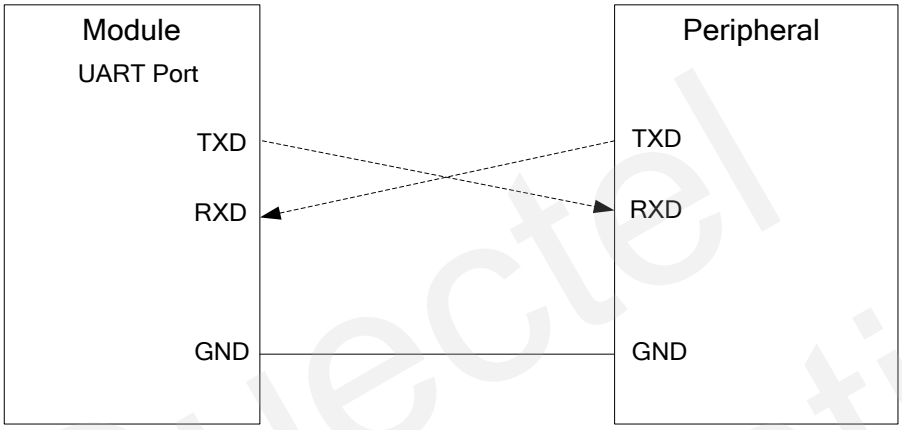

Figure 16: Reference Design for UART Port

3.6.1.3. Firmware Upgrade

The UART Port can be used for firmware upgrade. The PWRKEY pin must be pulled down before firmware upgrade. The following cautions must be taken into account.

- VBAT voltage must be stable
- PWRKEY pin must be set low

The following figure shows a reference design for UART port when it is used for firmware upgrade.

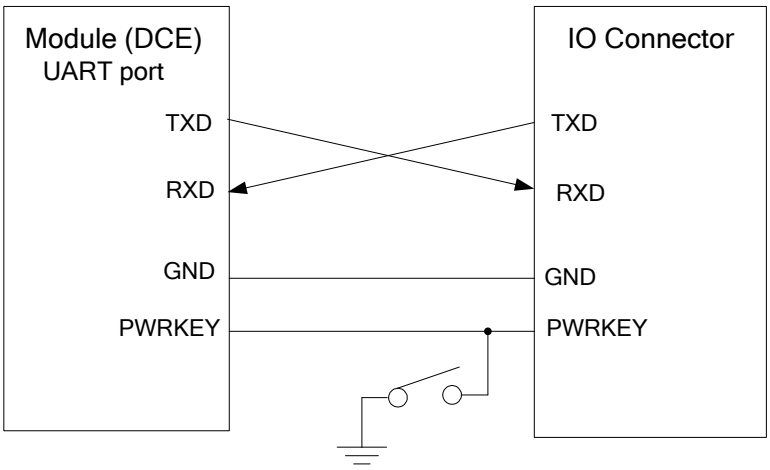

Figure 17: UART Port Reference Design for Firmware Upgrade

3.6.2. Debug Port

The Debug Port has two working modes (Basic Mode and Advanced Mode) which can be switched through configuring APP software.

- Under Basic Mode, the port can be used to execute software debugging and it can also be connected to a peripheral device. Its default baud rate is 115200bps.
- Under Advanced Mode, the port can only be used to execute software debugging, capture the system's log with Cather tool and call **QI_Debug_Trace()** to output the application log. In this mode, its baud rate is 460800bps.

A reference design for the Debug Port is shown as below.

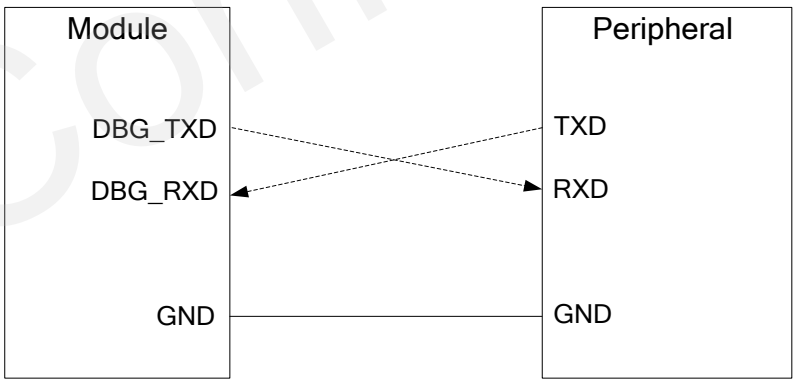

Figure 18: Reference Design for Debug Port

3.6.3. Auxiliary UART Port

Auxiliary UART Port:

- 8 data bits, no parity bit, one stop bit.
- Supported baud rates are as below:
  1200, 2400, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800bps.
- The default baud rate is 115200bps.

A reference design for Auxiliary UART Port is shown as below.

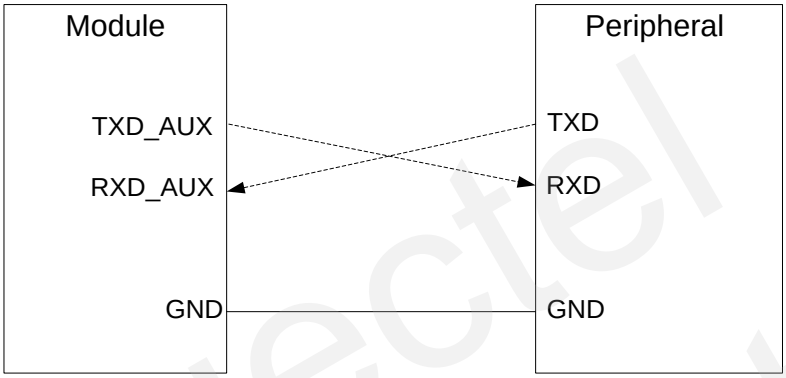

Figure 19: Reference Design for Auxiliary UART Port

3.6.4. UART Application

A reference design for 3.3V level match is shown as below. If the peripheral is a 3V system, please change the 5.6K resistors to 10K ones.

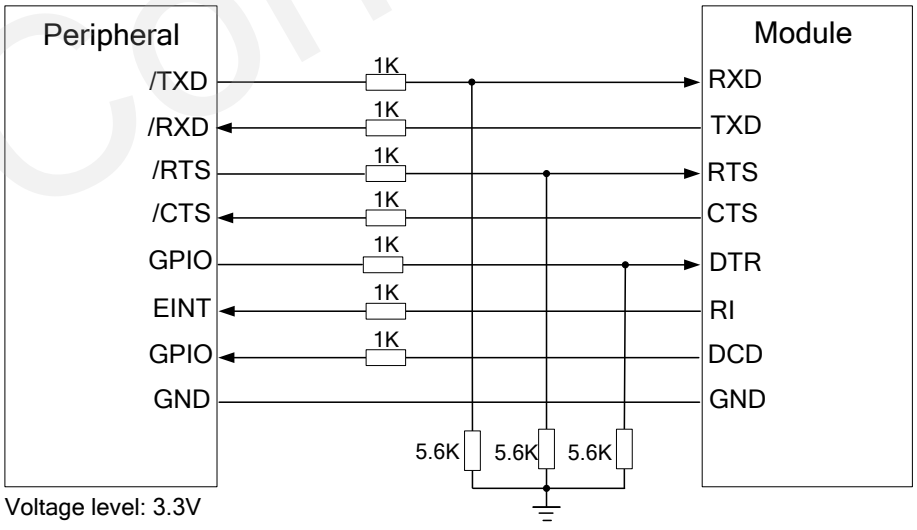

Figure 20: Level Match Design for 3.3V System

NOTE

It is highly recommended to add the resistor divider circuit on the UART signal lines when the host's voltage level is 3V or 3.3V. For systems with a higher voltage level, a level shifter IC could be used between the host and the module. For more details about UART circuit design, please refer to the ***document [14]***.

The following figure shows a sketch map between the module and standard RS-232 interface. As the electrical level of the module is 2.8V, a RS-232 level shifter must be used. Please make sure the I/O voltage of the level shifter which is connected to the module is 2.8V.

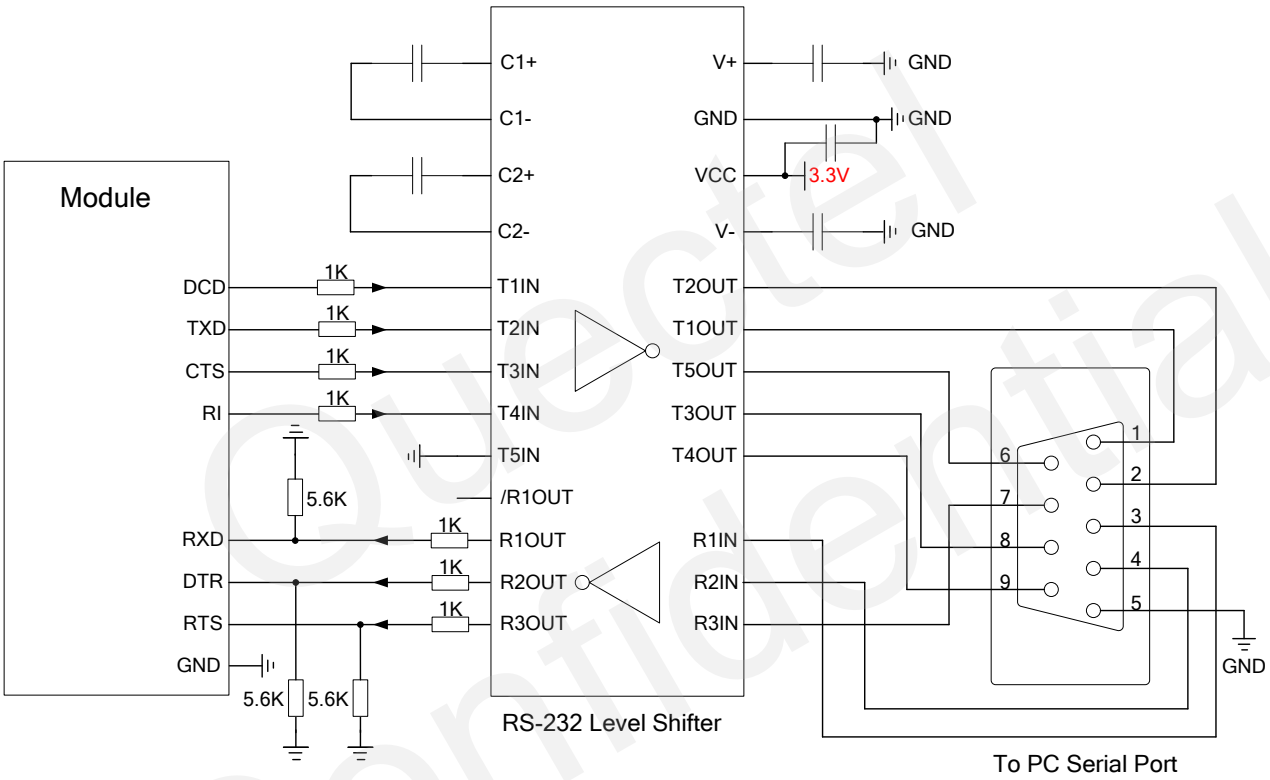

Figure 21: Sketch Map for RS-232 Interface Match

Please visit vendor's website to select a proper IC, such as: http://www.maximintegrated.com and http://www.exar.com/.

3.7. Audio Interfaces

The module provides one analog audio input channel and two analog audio output channels.

Table 9: Pin Definition of Audio Interfaces

Interface	Pin Name	Pin No.	Description
AIN/AOUT1	MICP	1	Microphone positive input
	MICN	2	Microphone negative input
	SPKP	3	Channel 1 audio positive output
	SPKN	4	Channel 1 audio negative output
AIN/AOUT2	AGND	5	Form a pseudo-differential pair with LOUDSPKP
	MICP	1	Microphone positive input
	MICN	2	Microphone negative input
	LOUDSPKP	52	Channel 2 Audio positive output
	LOUDSPKN	51	Channel 2 Audio negative output

Features of the two audio interfaces are listed below:

- AIN are used for input of microphone or line. An electret microphone is usually used. AIN are differential input channels.
- AOUT1 is used for output of the receiver. This channel is typically used for building a receiver into a handset. AOUT1 channel is a differential channel.
- AOUT2 is used for loudspeaker output as it is embedded with an amplifier of class AB whose maximum drive power is 870mW. AOUT2 is a differential channel.
- AOUT2 also can be used for output of earphone, and can be used as a single-ended channel. LOUDSPKP and AGND can establish a pseudo differential mode.
- Select the audio channel with command **AT+QAUDCH**.
- Adjust the input gain of the microphone with command **AT+QMIC**.
- Adjust the output gain for receiver or speaker with command **AT+CLVL**.
- Configure the parameters of echo cancellation function with command **AT+QECHO**.
- Configure the side tone gain with command **AT+QSIDET**.

Use command **AT+QAUDCH** to select audio channel:

- 0--AIN/AOUT1, the default value is 0.
- 1--AIN/AOUT2, this channel is always used for earphone.
- 2--AIN/AOUT2, this channel is always used for loudspeaker.

Table 10: AOUT2 Output Characteristics

Item	Condition	Min.	Typ.	Max.	Unit
RMS Power	8ohm load VBAT=4.2V THD+N=1%		870		mW
	8ohm load VBAT=3.3V THD+N=1%		530		mW

3.7.1. Decrease TDD Noise and Other Noise

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10pF and 33pF) for filtering out RF interference, thus reducing TDD noise. The 33pF capacitor is applied for filtering out 900MHz RF interference when the module is transmitting at EGSM900MHz. Without placing this capacitor, TDD noise could be heard. The 10pF capacitor here is used for filtering out 1800MHz RF interference. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out GSM850MHz, EGSM900MHz, DCS1800MHz and PCS1900MHz separately.

The severity degree of the RF interference in the voice channel during GSM transmitting period largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, you can choose a suitable capacitor based on the test results. Sometimes, even no RF filtering capacitor is required.

The capacitor which is used for filtering out RF noise should be close to audio interfaces, and the audio trace should be as short as possible.

In order to decrease radio or other signal interference, the position of RF antenna should be kept away from the audio interface and audio trace. The power trace could not be parallel with the audio trace, and should be far away from it.

The differential audio traces must be routed according to the differential signal layout rule.

3.7.2. Microphone Interfaces Design

AIN channel comes with internal bias supply for external electret microphone. A reference circuit is shown in the following figure.

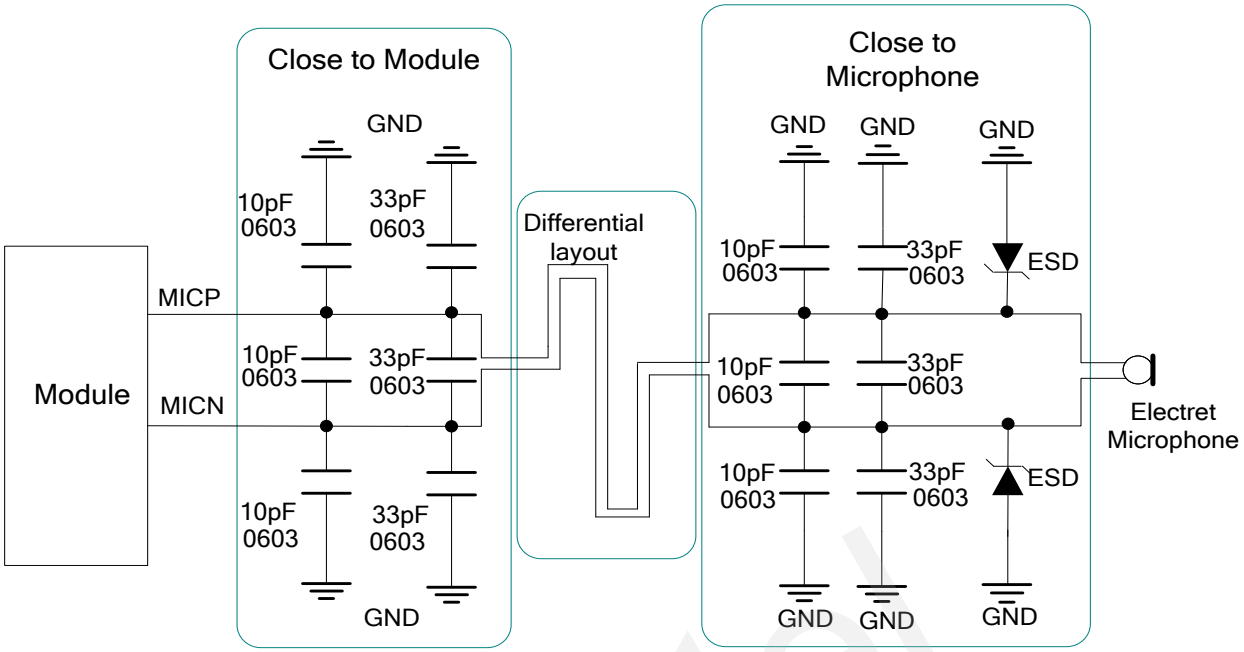

Figure 22: Reference Design for AIN

3.7.3. Receiver and Speaker Interface Design

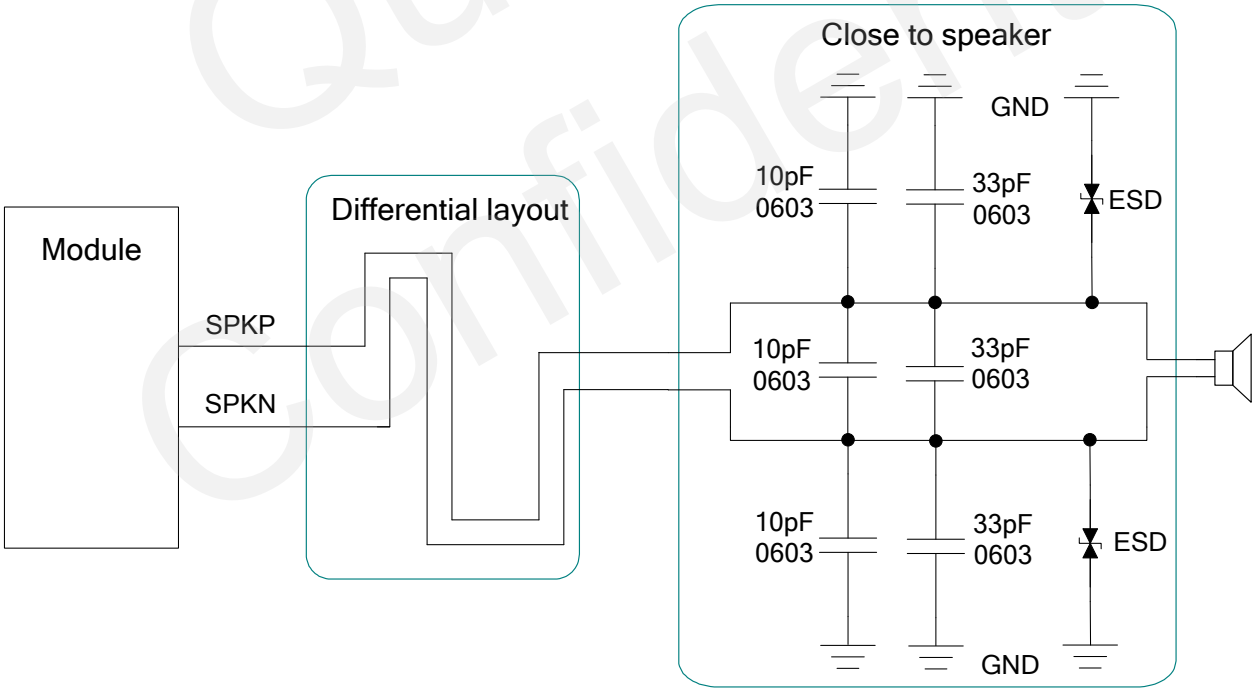

Figure 23: Handset Interface Design for AOUT1

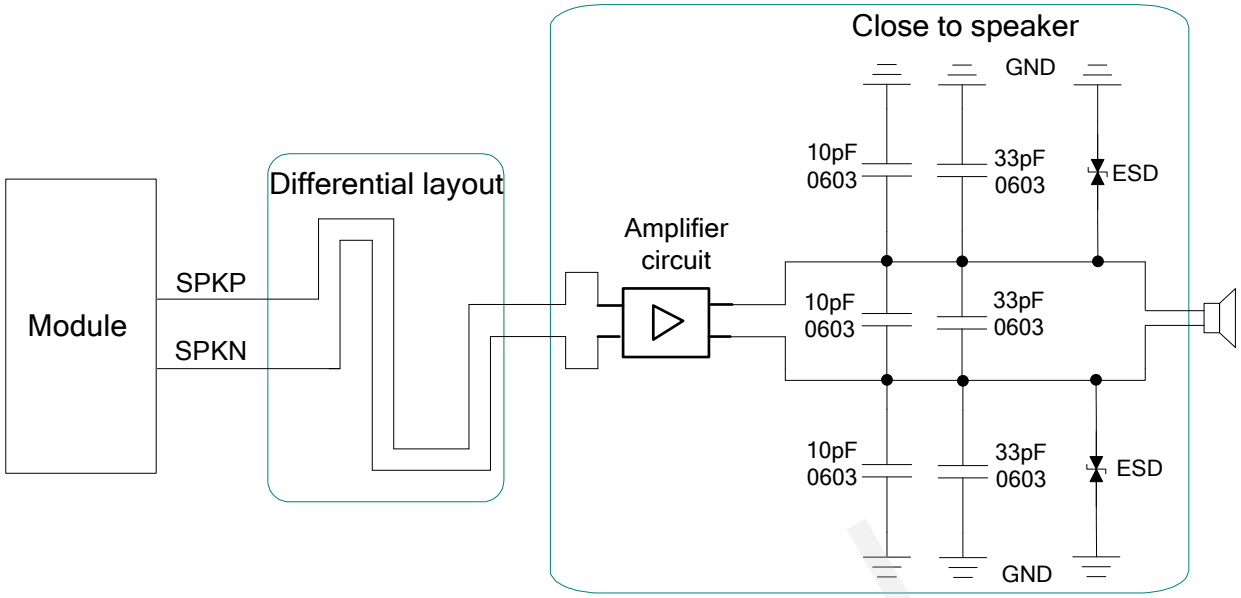

Figure 24: Speaker Interface Design with an Amplifier for AOUT1

A suitable differential audio amplifier can be chosen from the Texas Instrument's website (http://www.ti.com/). There are also other excellent audio amplifier vendors in the market.

3.7.4. Earphone Interface Design

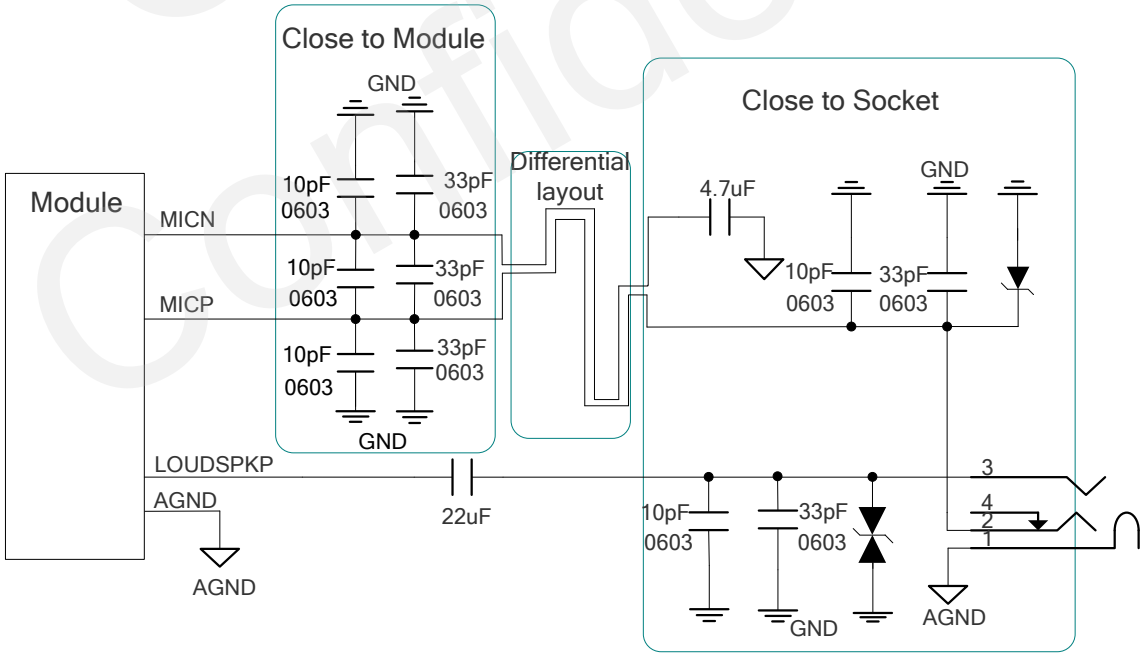

Figure 25: Earphone Interface Design

3.7.5. Loud Speaker Interface Design

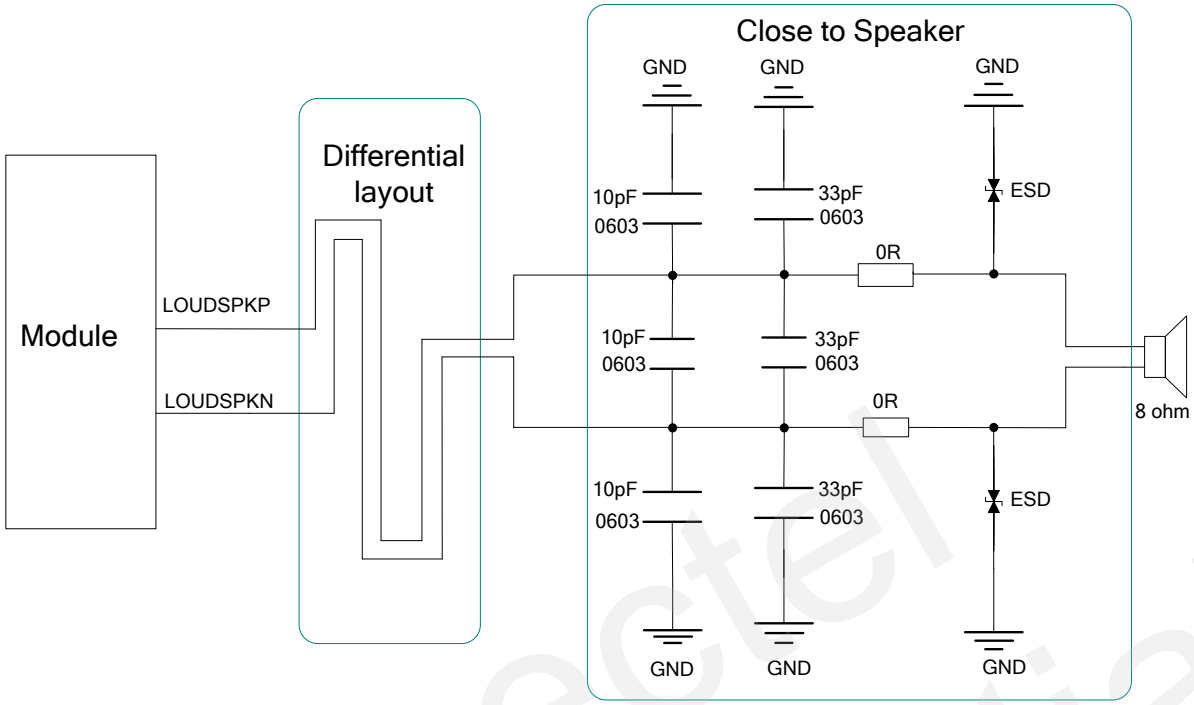

Figure 26: Loud Speaker Interface Design

3.7.6. Audio Characteristics

Table 11: Typical Electret Microphone Characteristics

Parameter	Min.	Typ.	Max.	Unit
Working Voltage	1.2	1.5	2.0	V
Working Current	200		500	uA
External Microphone Load Resistance		2.2		k Ohm

Table 12: Typical Speaker Characteristics

Parameter			Min.	Typ.	Max.	Unit
AOUT1 Output	Single-ended	Load resistance		32		Ohm
		Reference level	0		2.4	Vpp

	Differential	Load resistance		32	Ohm
		Reference level	0	4.8	Vpp
AOUT2 Output	Differential	Load resistance		8	Ohm
		Reference level	0	2×VBAT	Vpp
	Single-ended	Load resistance		8	Ohm
		Reference level	0	VBAT	Vpp

3.8. SIM Card Interface

The SIM interface supports the functionality of the GSM Phase 1 specification and also supports the functionality of the new GSM Phase 2+ specification for FAST 64kbps SIM card (intended for use with a SIM application Tool-kit).

The SIM interface is powered by an internal regulator in the module. Both 1.8V and 3.0V SIM cards are supported. Dual SIM dual standby function is supported.

Table 13: Pin Definition of SIM Interface

Pin Name	Pin No.	Description	Alternate Function[1)]
SIM1_VDD	11	Supply power for SIM card. Automatic detection of SIM1 card voltage. 3.0V±5% and 1.8V±5%. Maximum supply current is around 10mA.	
SIM1_CLK	10	SIM1 card clock	
SIM1_DATA	8	SIM1 card data I/O	
SIM1_RST	9	SIM1 card reset	
SIM1_PRESENCE	34	SIM1 card detection	DTR
SIM_GND	12	SIM1 card ground	
SIM2_VDD	17	Supply power for SIM card. Automatic detection of SIM2 card voltage. 3.0V±5% and 1.8V±5%. Maximum supply current is around 10mA.	
SIM2_CLK	18	SIM2 card clock	

SIM2_DATA	20	SIM2 card data I/O
SIM2_RST	19	SIM2 card reset

NOTE

[1] If several interfaces share the same I/O pin, to avoid conflict between these alternate functions, only one peripheral should be enabled at a time.

The following figure is a reference design for SIM1 interface.

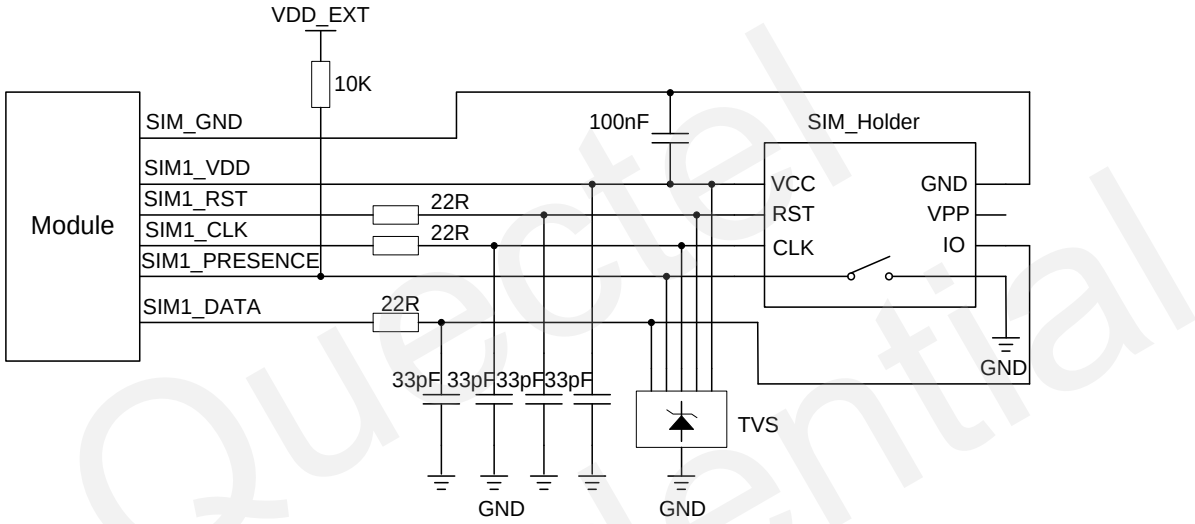

Figure 27: Reference Circuit for SIM1 Interface with an 8-pin SIM Card Holder

If SIM1 card detection function is not used, keep SIM1_PRESENCE pin open. A reference circuit for a 6-pin SIM card holder is illustrated below.

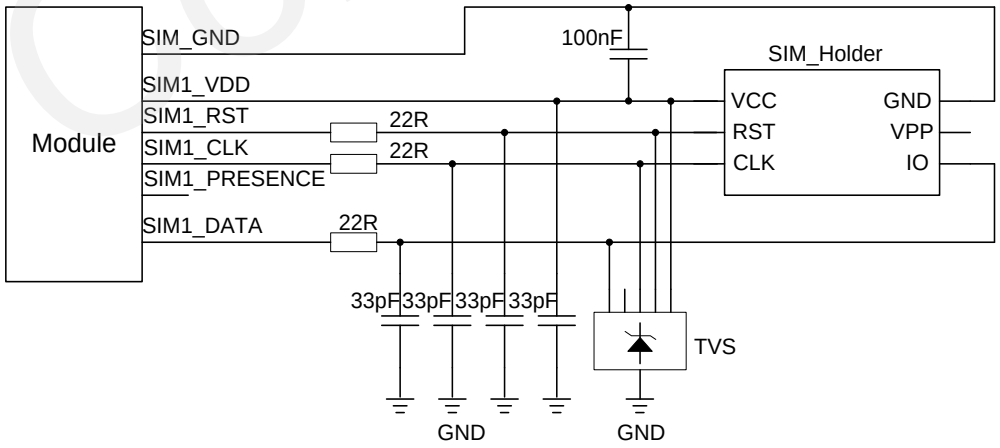

Figure 28: Reference Circuit for SIM1 Interface with a 6-pin SIM Card Holder

The following figure is a reference design for SIM2 interface with a 6-pin SIM card holder.

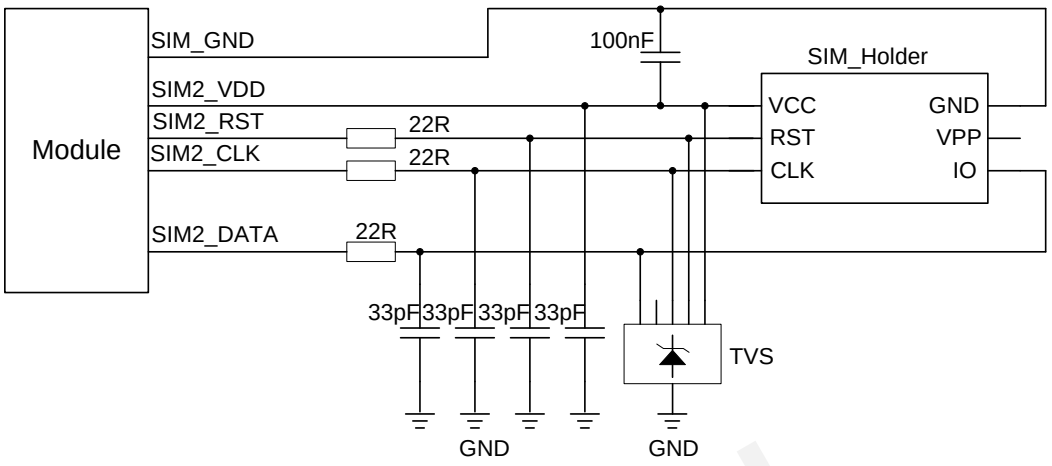

Figure 29: Reference Circuit for SIM2 Interface with a 6-pin SIM Card Holder

For more information of SIM card holder, you can visit http://www.amphenol.com and http://www.molex.com.

In order to enhance the reliability and availability of the SIM card in the customer's application, please follow the following rules in the SIM card circuit design.

- Keep layout of SIM card as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep SIM card signal away from RF and VBAT traces.
- Assure the ground between module and SIM card holder short and wide. Keep the width of ground no less than 0.5mm to maintain the same electric potential. The decouple capacitor of SIM_VDD is less than 1uF and must be near to SIM card holder.
- To avoid cross-talk between SIM_DATA and SIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array. For more information of TVS diode, please visit http://www.onsemi.com. The most important rule is to place the ESD protection device close to the SIM card holder and make sure the SIM card interface signal lines being protected will go through the ESD protection device first and then lead to the module. The 22Ω resistors should be connected in series between the module and the SIM card so as to suppress EMI spurious transmission and enhance ESD protection. Please note that the SIM peripheral circuit should be close to the SIM card holder.
- Place the RF bypass capacitors (33pF) close to the SIM card on all signal lines for improved EMI suppression.

3.9. SD Card Interface

The module provides an SD card interface that supports many types of memory, such as Memory Stick, SD/MCC card, and T-Flash or Micro SD card. The following are the main features of SD card interface.

- Only support 1bit serial mode
- Not support the SPI mode for SD memory card
- Not support multiple SD memory cards
- Not support hot plug
- The data rate up to 48MHz in serial mode
- Up to 32GB maximum memory card capacity

With the SD card interface features and reference circuit shown as below, you can easily design the SD card application circuit to enhance the memory capacity of the module. Users can store some high-capacity files to external memory card. For instance, in automotive application systems, the module can record and store the audio file to the SD card, and also can play the audio files in SD card.

Table 14: Pin Definition of SD Card Interface

Pin Name	Pin No.	Description
SD_CMD	16	Command signal of SD card output
SD_CLK	14	Clock signal of SD card output
SD_DATA	15	Data output and input signal of SD card

A reference design for micro SD card is shown below.

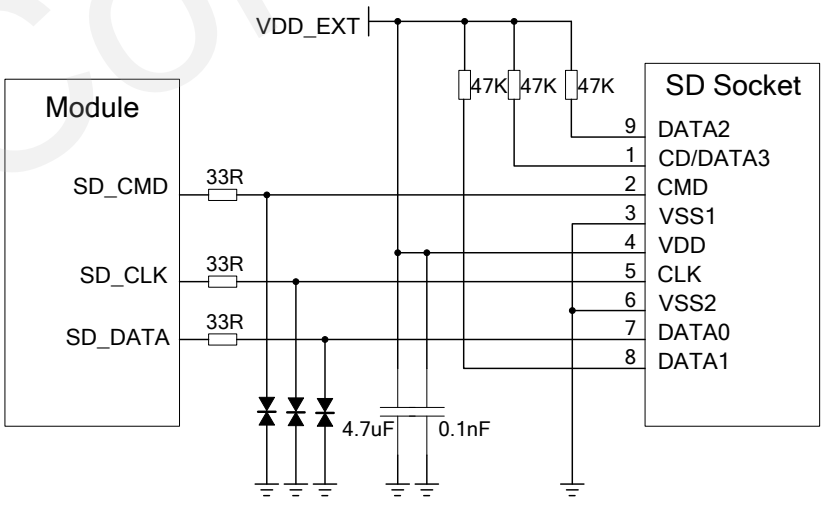

Figure 30: Reference Circuit for Micro SD Card

Table 15: Pin Definition of SD Card Interface

Pin No.	Pin Name of SD Card	Pin Name of T-Flash (Micro SD) Card
1	CD/DATA3	DATA2
2	CMD	CD/DATA3
3	VSS1	CMD
4	VDD	VDD
5	CLK	CLK
6	VSS2	VSS
7	DATA0	DATA0
8	DATA1	DATA1
9	DATA2	

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- Keep all the SD card signals far away from VBAT power and RF trace.
- Route all SD card signals as short as possible. Ensure the length of every trace does not exceed 10cm.
- The SD_CLK, SD_DATA and SD_CMD trace should be routed together. Make sure the trace length difference among SD_DATA, SD_CMD and SD_CLK is less than 10mm.
- In order to offer good ESD protection, it is recommended to add TVS on signals with capacitance less than 15pF.
- Reserve external pull-up resistors for other data lines except the DATA0 signal.
- SD_CLK and SD_DATA lines must be shielded by ground so as to improve EMI suppression capability.

3.10. PCM Interface

M66-DS-OpenCPU provides a PCM interface which is used for digital audio transmission between the module and the device. The interface is composed of PCM_CLK, PCM_SYNC, PCM_IN and PCM_OUT signal lines.

Pulse-code modulation (PCM) is a converter that changes the consecutive analog audio signals to discrete digital signals. The whole procedure of pulse-code modulation contains sampling, quantizing and

encoding.

Table 16: Pin Definition of PCM Interface

Pin Name	Pin No.	Description
PCM_CLK	35	PCM clock output
PCM_SYNC	36	PCM frame synchronization output
PCM_IN	37	PCM data input
PCM_OUT	38	PCM data output

NOTE

If the PCM function is not used, these pins can be used as GPIOs. For detailed information about GPIO, please refer to ***Chapter 3.15***.

3.10.1. Parameter Configuration

M66-DS-OpenCPU module supports 16-bit linear code PCM format. The sample rate is 8KHz and the clock source is 256KHz. The module can only act in master mode. The PCM interface supports both long and short frame synchronization, and it only supports MSB first. For more detailed information, please refer to the table below.

Table 17: PCM Parameter Configuration

Parameter	Description
Interface Format	Linear
Data Length	Linear: 16 bits
Sample Rate	8KHz
PCM Clock/Synchronization Source	Module acts in master mode: clock and synchronization sources are generated by module
PCM Synchronization Rate	8KHz
PCM Clock Rate	Module acts master mode: 256 KHz (linear)
PCM Synchronization Format	Long/short frame synchronization

PCM Data Ordering	MSB first
Zero Padding	Not supported
Sign Extension	Not supported

3.10.2. Timing Diagram

The sample rate of the PCM interface is 8KHz and the clock source rate is 256KHz. Every frame contains 32-bit data. M66-DS-OpenCPU supports 16-bit linear code PCM format. The left 16 bits are valid, and the data of the left 16 bits and the right 16 bits are the same. The following are the timing diagram of different frame synchronization formats.

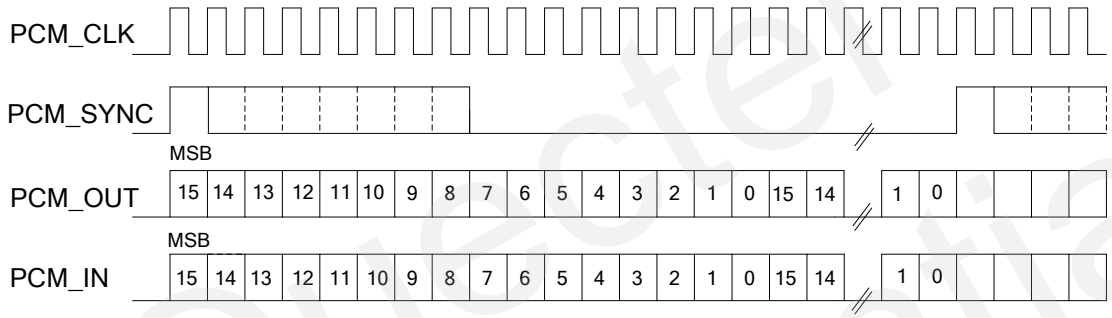

Figure 31: Timing Diagram for Long Frame Synchronization

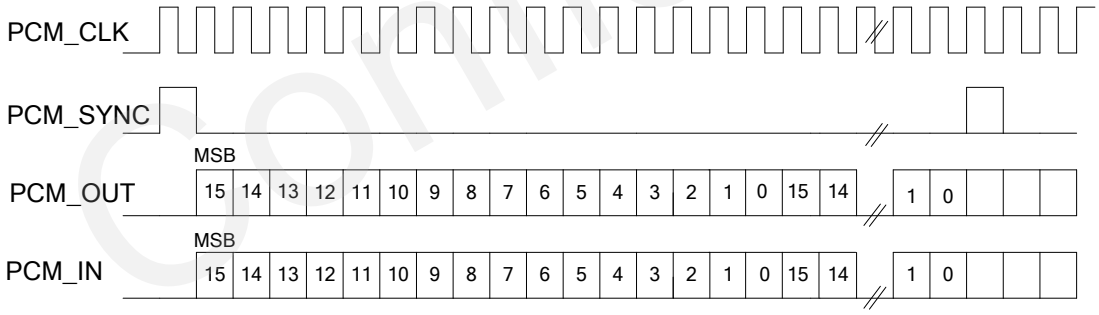

Figure 32: Timing Diagram for Short Frame Synchronization

3.10.3. Reference Design

M66-DS-OpenCPU can only act as a master, providing clock and synchronization source for PCM bus. A reference design for PCM is shown as below.

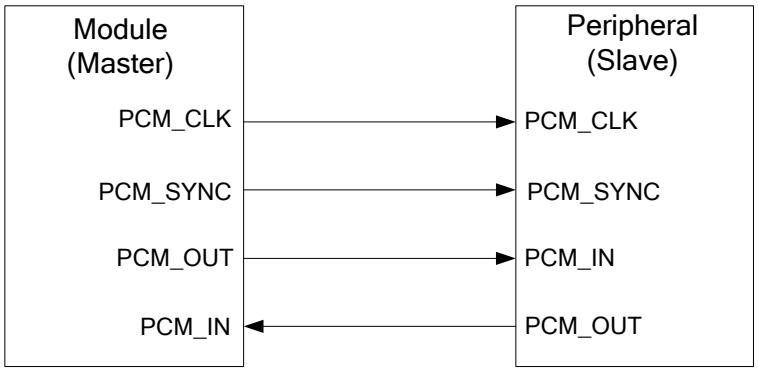

Figure 33: Reference Design for PCM

3.10.4. AT Command

There are two AT commands available for PCM configuration. The details are listed below.

- **AT+QPCMON** is used to configure the operating mode of PCM.

Command format: **AT+QPCMON=mode, Sync_Type, Sync_Length, SignExtension, MSBFirst**.

Table 18: AT+QPCMON Command Description

Parameter	Value Range	Description
Mode	0~2	0: Close PCM 1: Open PCM 2: Open PCM when audio talk is set up
Sync_Type	0~1	0: Short frame synchronization 1: Long frame synchronization
Sync_Length	1~8	Programmable from one bit to eight bits via firmware configuration in long frame synchronization format
SignExtension	0~1	Not supported
MSBFirst	0~1	0: MSB first 1: Not supported

- **AT+QPCMVOL** is used to configure the input and output volume of PCM.

Command format: **AT+QPCMVOL=vol_pcm_in, vol_pcm_out**

Table 19: AT+QPCMVOL Command Description

Parameter	Value Range	Description
vol_pcm_in	0~32767	Set the input volume
vol_pcm_out	0~32767	Set the output volume The voice may be distorted when the value exceeds 16384.

3.11. SPI and I2C Interfaces

M66-DS-OpenCPU module supports both SPI and I2C interfaces.

3.11.1. SPI Interface

The SPI interface is multiplexed by PCM interface. SPI interface of M66-DS-OpenCPU acts as the master only. It provides a duplex, synchronous and serial communication link with the peripheral devices. Its operation voltage is 2.8V, with clock rates up to 10MHz. Main features of the SPI interface are listed below.

- Support master mode operation
- Adjustable clock speed
- Serial clock with programmable polarity and phase

The logic levels of SPI interface are described in the following table.

Table 20: Logic Levels of SPI Interface

Parameter	Min.	Max.	Unit
V_{IL}	0	0.25×VDD_EXT	V
V_{IH}	0.75×VDD_EXT	VDD_EXT +0.2	V
V_{OL}	0	0.15×VDD_EXT	V
V_{OH}	0.85×VDD_EXT	VDD_EXT	V

Table 21: Pin Definition of SPI Interface

Pin No.	Name	Description	Alternate Function[1)]
38	SPI_MOSI	Master output, Slave input of SPI Interface	PCM_OUT
37	SPI_CLK	Clock signal of SPI interface	PCM_IN
36	SPI_MISO	Master input, Slave output of SPI Interface	PCM_SYNC
35	SPI_CS	Chip select of SPI Interface	PCM_CLK

NOTE

1) If several interfaces share the same I/O pin, to avoid conflict between these alternate functions, only one peripheral should be enabled at a time.

The M66-DS-OpenCPU SPI must be configured as the master. The API functions of the file system can be used to read/write SPI. For detailed information about the software design, please refer to the ***document [12]***.

3.11.2. I2C Interface

I2C is a two-wire serial interface which is multiplexed by RI and DCD pins. The two signals are SCL and SDA. Main features of the I2C interface are listed below.

- Support master mode operation
- Adjustable clock speed for LS/FS mode operation
- Support 7-bit addressing
- Support high speed mode

Table 22: Logic Levels of I2C Interface

Parameter	Min.	Max.	Unit
V_{IL}	0	0.25×VDD_EXT	V
V_{IH}	0.75×VDD_EXT	VDD_EXT +0.2	V
V_{OL}	0	0.15×VDD_EXT	V
V_{OH}	0.85×VDD_EXT	VDD_EXT	V

Table 23: Pin Definition of I2C Interface

Pin No.	Name	Description	Comment	Alternate Function[1)]
33	I2C_SCL	I2C serial clock	Require an external pull-up resistor	RI
32	I2C_SDA	I2C serial data		DCD

NOTE

[1)] If several interfaces share the same I/O pin, to avoid conflict between these alternate functions, only one peripheral should be enabled at a time.

The API functions of the file system can be used to read/write I2C. For detailed information about the software design, please refer to the ***document [12]***.

3.12. ADC

The module provides an ADC input channel to measure the value of voltage. The API function **QI_ADC_Sampling()** can be used to read the voltage value from ADC input channel. For detailed information about the software design, please refer to the ***document [12]***.

Table 24: Pin Definition of the ADC

Pin Name	Pin No.	Description
ADC0	7	Analog to digital converter.

Table 25: Characteristics of the ADC

Item	Min.	Typ.	Max.	Unit
Voltage Range	0		2.8	V
ADC Resolution		10		bits
ADC Accuracy		2.7		mV

NOTE

If the voltage value from ADC input channel is greater than 2.8V, it will be read as 2.8V only by **Ql_ADC_Sampling()**. So you need to keep the voltage value of ADC less than 2.8V through using a voltage divider.

3.13. External Interrupt

M66-DS-OpenCPU module possesses one external interrupt which supports level trigger. The external interrupt is a multiplexed function. When the default function of pin 34 is not used, it can be configured as external interrupt.

Table 26: Pin List for External Interrupt

Pin No.	Pin Name	Trigger Type
34	DTR	Level

If an external interrupt occurs, the previously registered interrupt callback function will be invoked. For detailed information about the software design, please refer to the ***document [12]***.

NOTE

If external interrupt is not used, the pin can be multiplexed as GPIO. For detailed information about GPIO, please refer to ***Chapter 3.15***.

3.14. PWM

M66-DS-OpenCPU module provides a PWM signal output channel which is called NETLIGHT. NETLIGHT indicates network status by default and it can also be configured by related API function. The working status of NETLIGHT is shown in the following table.

Table 27: Working Status of NETLIGHT

State	Module Function
OFF	The module is not running.
64ms ON/800ms OFF	The module is not synchronized with network.
64ms ON/2000ms OFF	The module is synchronized with network.
64ms ON/600ms OFF	GPRS data transmission.

A reference design for NETLIGHT is shown as below.

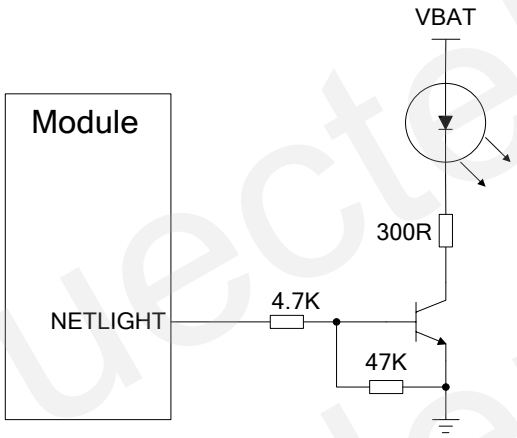

Figure 34: Reference Design for NETLIGHT

PWM signal parameters can be configured by calling the API function **Ql_PWM_Output()**. For detailed information about software design, please refer to the ***document [12]***.

3.15. GPIO

M66-DS-OpenCPU module provides 12 GPIOs in all. In order to reduce the pin number, GPIO is multiplexed with other functions. When the pin's default function is not used, it can be configured as GPIO. API functions, such as **Ql_GPIO_Init**, **Ql_GPIO_SetLevel**, **Ql_GPIO_SetDirection**, and **Ql_GPIO_SetPullSelection**, can be used for GPIO operation. For detailed information about the software design, please refer to the ***document [12]***.

Table 28: Pin List for GPIO

Pin No.	Name	Mode	Reset		Output Driving
			I/O	PU/PD	
23	NETLIGHT	Mode 2	I	PD	4mA
34	DTR	Mode 2	I	PD	4mA
33	RI	Mode 2	I	PD	4mA
32	DCD	Mode 2	I	PD	4mA
31	CTS	Mode 2	I	PU	4mA
30	RTS	Mode 2	I	PU	4mA
25	RXD_AUX	Mode 2	I	PD	4mA
24	TXD_AUX	Mode 2	I	PD	4mA
35	PCM_CLK	Mode 2	HO	-	4mA
36	PCM_SYNC	Mode 2	I	PD	4mA
37	PCM_IN	Mode 2	I	PU	4mA
38	PCM_OUT	Mode 2	I	PD	4mA

If you configure GPIO as input or output port, please pay attention to level match when the module is connected with other peripherals. A reference design for 3.3V level match is shown as below.

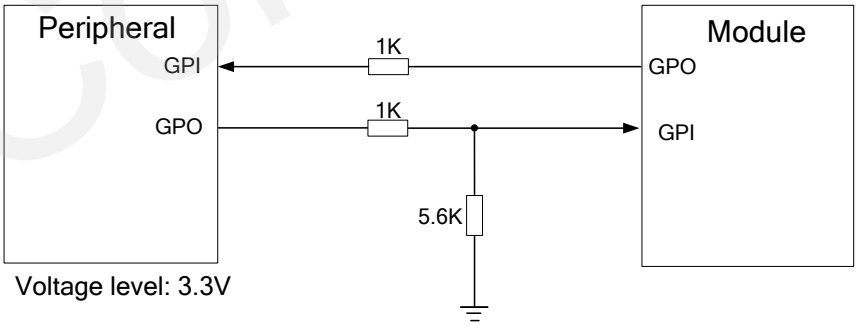

Figure 35: GPIO Level Match Design for 3.3V System

NOTE

If the digital I/O between customer and module does not match, it will cause some unexpected results. So it is highly recommended to add the level match circuit when the module is connected with other peripherals. For more details about digital I/O application, please refer to the ***document [14]***.

3.16. RF Transmission Signal Indication

M66-DS-OpenCPU module provides a RFTXMON pin which will rise when the transmitter is active and fall after the transmitter activity is completed.

Table 29: Pin Definition of the RFTXMON

Pin Name	Pin No.	Description
RFTXMON	26	RF transmission signal indication

There are two different operation modes for this function:

1. Active during the TX Activity

RFTXMON pin is used to indicate the TX burst. When it outputs a high level, 220us later there will be a TX burst.

You can execute **AT+QCFG="RFTXburst", 1** to enable the function. The timing of the RFTXMON signal is shown below.

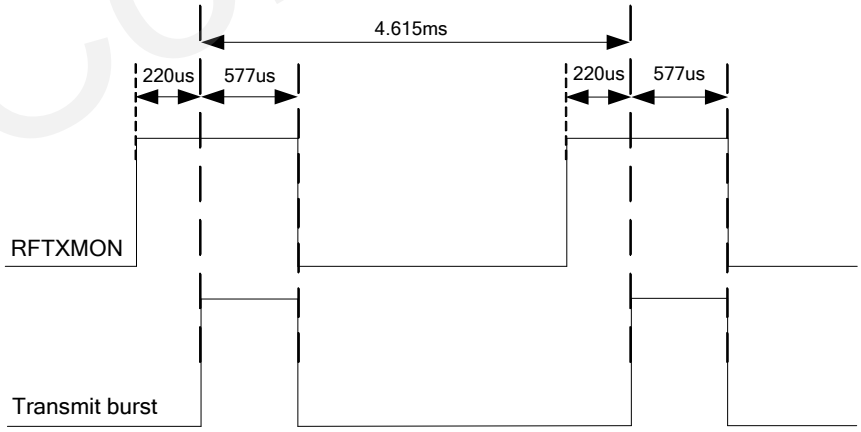

Figure 36: RFTXMON Signal during Burst Transmission

2. Active during the Call

RFTXMON will be HIGH during a call and then will become LOW after the call is hanged up.

You can execute **AT+QCFG="RFTXburst", 2** to enable the function. The timing of the RFTXMON signal is shown below.

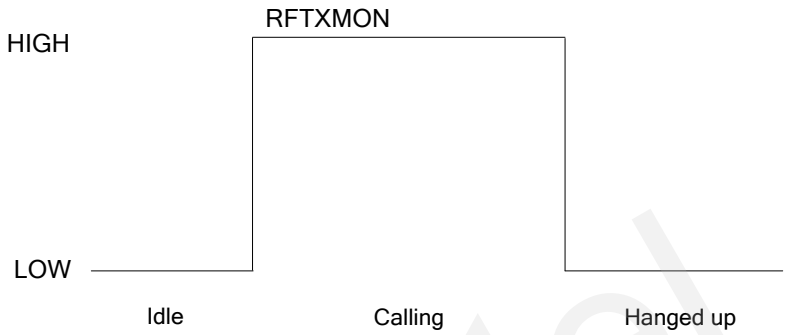

Figure 37: RFTXMON Signal during Calling

4 Antenna Interfaces

M66-DS-OpenCPU has two antenna interfaces: GSM antenna and BT antenna interfaces. The pin 28 is the Bluetooth antenna pad. The pin 40 is the GSM antenna pad. The RF interface of the two antenna pads has an impedance of 50Ω.

4.1. GSM Antenna Interface

There is a GSM antenna pad named RF_ANT for M66-DS-OpenCPU.

Table 30: Pin Definition of the RF_ANT

Name	Pin	Description
GND	39	Ground
RF_ANT	40	GSM antenna pad
GND	41	Ground
GND	42	Ground

4.1.1. Reference Design

The external antenna must be matched properly to achieve the best performance, so a matching circuit is necessary. A reference design for RF_ANT is shown as below.

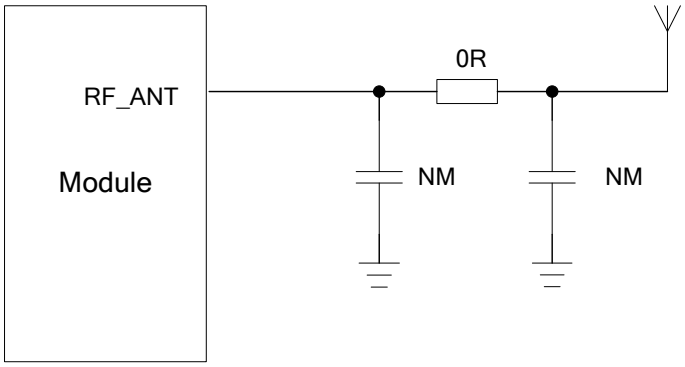

Figure 38: Reference Design for GSM Antenna Connection

M66-DS-OpenCPU provides an RF antenna pad for antenna connection. The RF trace in host PCB connected to the module RF antenna pad should be coplanar waveguide line or microstrip line, and its characteristic impedance should be close to 50Ω. M66-DS-OpenCPU comes with grounding pads which are next to the antenna pad in order to give a better grounding system. Additionally, a π type matching circuit is suggested to be used to adjust the RF performance.

To minimize the loss on RF trace and RF cable, please pay attention to the antenna design. The following tables show the requirements on GSM antenna.

Table 31: Antenna Cable Requirements

Type	Requirements
GSM850/EGSM900	Cable insertion loss <1dB
DCS1800/PCS1900	Cable insertion loss <1.5dB

Table 32: Antenna Requirements

Type	Requirements
Frequency Range	Depend on frequency band(s) provided by the network operator
VSWR	≤ 2
Gain (dBi)	1
Max Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Vertical

4.1.2. RF Output Power

Table 33: RF Output Power

Frequency	Max.	Min.
GSM850	33dBm±2dB	5dBm±5dB
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 2.5dB. This design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

4.1.3. RF Receiving Sensitivity

Table 34: RF Receiving Sensitivity

Frequency	Receiving Sensitivity
GSM850	< -109dBm
EGSM900	< -109dBm
DCS1800	< -109dBm
PCS1900	< -109dBm

4.1.4. Operating Frequencies

Table 35: Operating Frequencies

Frequency	Receiving	Transmitting	ARFCH
GSM850	869~894MHz	824~849MHz	128~251
EGSM900	925~960MHz	880~915MHz	0~124, 975~1023

DCS1800	1805~1880MHz	1710~1785MHz	512~885
PCS1900	1930~1990MHz	1850~1910MHz	512~810

4.1.5. RF Cable Soldering

Soldering the RF cable to RF pad of module correctly will reduce the loss on the path of RF. Please refer to the following example for RF cable soldering.

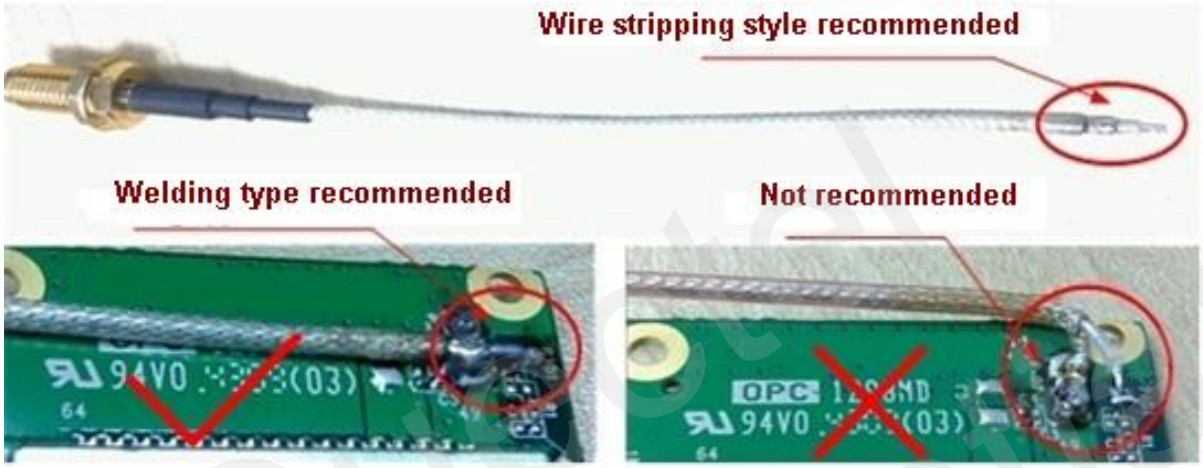

Figure 39: RF Cable Soldering Sample

4.2. Bluetooth Antenna Interface

M66-DS-OpenCPU supports Bluetooth function. Bluetooth is a wireless technology that allows devices to communicate or transmit data or voice wirelessly over a short distance. It is described as a short-range communication technology intended to replace the cables connecting portable and/or fixed devices while maintaining a high level of security. Bluetooth is standardized as IEEE802.15 and operates in the 2.4 GHz range using RF technology. Its data rate is up to 3Mbps.

M66-DS-OpenCPU is fully compliant with Bluetooth specification 3.0. It supports SPP profile.

The module provides a Bluetooth antenna pad named BT_ANT.

Table 36: Pin Definition of the BT_ANT

Name	Pin	Description
BT_ANT	28	BT antenna pad
GND	29	Ground

The external antenna must be matched properly to achieve the best performance, so a matching circuit is necessary. The connection is recommended as the following figure.

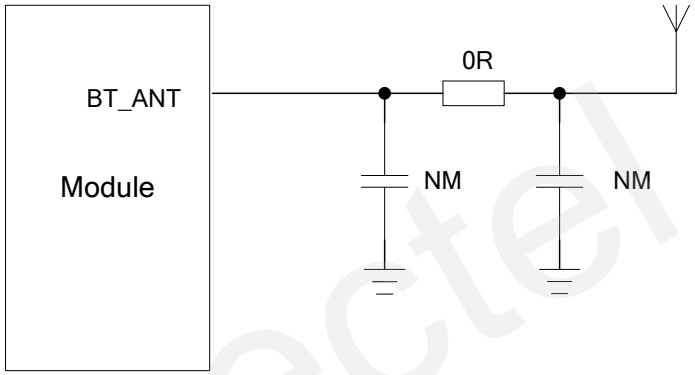

Figure 40: Reference Design for Bluetooth Antenna Connection

There are some suggestions for placing components and RF trace lying for Bluetooth antenna interface:

- Antenna matching circuit should be close to the antenna;
- Assure the RF trace has an impedance of 50Ω;
- The RF traces should be kept far away from the high frequency signals and strong disturbing sources.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 37: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	+4.73	V
Peak Current of Power Supply	0	2	A
RMS Current of Power Supply (during one TDMA-frame)	0	0.7	A
Voltage at Digital Pins	-0.3	3.08	V
Voltage at Analog Pins	-0.3	3.08	V
Voltage at Digital/Analog Pins in Power-down Mode	-0.25	0.25	V

5.2. Operating Temperature

The operating temperature is listed in the following table.

Table 38: Operating Temperature

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range	-35	+25	+75	ºC
Extended Temperature Range	-40		+85	ºC

NOTES

1. Within operation temperature range, the module is 3GPP compliant.
2. Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP compliant again.

5.3. Power Supply Ratings

Table 39: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	Supply voltage	Voltage must stay within the min/max values, including voltage drop, ripple, and spikes.	3.3	4.0	4.6	V
	Voltage drop during burst transmission	Maximum power control level on GSM850 and EGSM900			400	mV
I_{VBAT}	Average supply current	Power down mode		150		uA
		SLEEP mode @DRX=5		1.3		mA
		Minimum functionality mode **AT+CFUN=0**				
		IDLE mode		13		mA

		SLEEP mode	0.98	mA
		AT+CFUN=4		
		IDLE mode	13	mA
		SLEEP mode	1.0	mA
		TALK mode		
		GSM850/EGSM900[1)]	174/175	mA
		DCS1800/PCS1900[2)]	153/151	mA
		DATA mode, GPRS (3Rx, 2Tx)		
		GSM850/EGSM900[1)]	363/356	mA
		DCS1800/PCS1900[2)]	234/257	mA
		DATA mode, GPRS (2Rx, 3Tx)		
		GSM850/EGSM900[1)]	496/487	mA
		DCS1800/PCS1900[2)]	305/348	mA
		DATA mode, GPRS (4Rx, 1Tx)		
		GSM850/EGSM900[1)]	216/222	mA
		DCS1800/PCS1900[2)]	171/169	mA
		DATA mode, GPRS (1Rx, 4Tx)		
		GSM850/EGSM900[1)]	470/471[3)]	mA
		DCS1800/PCS1900[2)]	377/439	mA
Peak supply current (during transmission slot)	Maximum power control level on GSM850 and EGSM900		1.6 2	A

NOTES

1. [1)] Power control level PCL 5.
2. [2)] Power control level PCL 0.
3. [3)] Under the GSM850 and EGSM900 spectrum, the power of 1Rx and 4Tx has been reduced.

5.4. Current Consumption

The values of current consumption are shown as below.

Table 40: Current Consumption

Condition	Current Consumption
Voice Call	
GSM850	@power level #5 <300mA, Typical 174mA @power level #12, Typical 83mA @power level #19, Typical 62mA
EGSM900	@power level #5 <300mA, Typical 175mA @power level #12, Typical 83mA @power level #19, Typical 63mA
DCS1800	@power level #0 <250mA, Typical 153mA @power level #7, Typical 73mA @power level #15, Typical 60mA
PCS1900	@power level #0 <250mA, Typical 151mA @power level #7, Typical 76mA @power level #15, Typical 61mA
GPRS Data	
DATA Mode, GPRS (3 Rx, 2Tx) CLASS 12	
GSM850	@power level #5 <550mA, Typical 363mA @power level #12, Typical 131mA @power level #19, Typical 91mA
EGSM900	@power level #5 <550mA, Typical 356mA @power level #12, Typical 132mA @power level #19, Typical 92mA
DCS1800	@power level #0 <450mA, Typical 234mA @power level #7, Typical 112mA @power level #15, Typical 88mA
PCS1900	@power level #0 <450mA, Typical 257mA @power level #7, Typical 119mA @power level #15, Typical 89mA
DATA Mode, GPRS (2 Rx, 3Tx) CLASS 12	
GSM850	@power level #5 <640mA, Typical 496mA @power level #12, Typical 159mA @power level #19, Typical 99mA

EGSM900	@power level #5 <600mA, Typical 487mA @power level #12, Typical 160mA @power level #19, Typical 101mA
DCS1800	@power level #0 <490mA, Typical 305mA @power level #7, Typical 131mA @power level #15, Typical 93mA
PCS1900	@power level #0 <480mA, Typical 348mA @power level #7, Typical 138mA @power level #15, Typical 94mA
DATA Mode, GPRS (4 Rx,1Tx) CLASS 12	
GSM850	@power level #5 <350mA, Typical 216mA @power level #12, Typical 103mA @power level #19, Typical 83mA
EGSM900	@power level #5 <350mA, Typical 222mA @power level #12, Typical 104mA @power level #19, Typical 84mA
DCS1800	@power level #0 <300mA, Typical 171mA @power level #7, Typical 96mA @power level #15, Typical 82mA
PCS1900	@power level #0 <300mA, Typical 169mA @power level #7, Typical 98mA @power level #15, Typical 83mA
DATA Mode, GPRS (1 Rx, 4Tx) CLASS 12	
GSM850	@power level #5 <600mA, Typical 470mA @power level #12, Typical 182mA @power level #19, Typical 106mA
EGSM900	@power level #5 <600mA, Typical 471mA @power level #12, Typical 187mA @power level #19, Typical 109mA
DCS1800	@power level #0 <500mA, Typical 377mA @power level #7, Typical 149mA @power level #15, Typical 97mA
PCS1900	@power level #0 <500mA, Typical 439mA @power level #7, Typical 159mA @power level #15, Typical 99mA

NOTE

GPRS Class 12 is the default setting. The module can be configured from GPRS Class 1 to Class 12. Setting to lower GPRS class would make it easier to design the power supply for the module.

5.5. Electrostatic Discharge

Although the GSM engine is generally protected against Electrostatic Discharge (ESD), ESD protection precautions should still be emphasized. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any applications using the module.

The measured ESD values of the module are shown as the following table.

Table 41: ESD Endurance (Temperature: 25ºC, Humidity: 45%)

Tested Point	Contact Discharge	Air Discharge
VBAT, GND	±5KV	±10KV
RF_ANT	±5KV	±10KV
TXD, RXD	±2KV	±4KV
Others	±0.5KV	±1KV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module.

6.1. Mechanical Dimensions of the Module

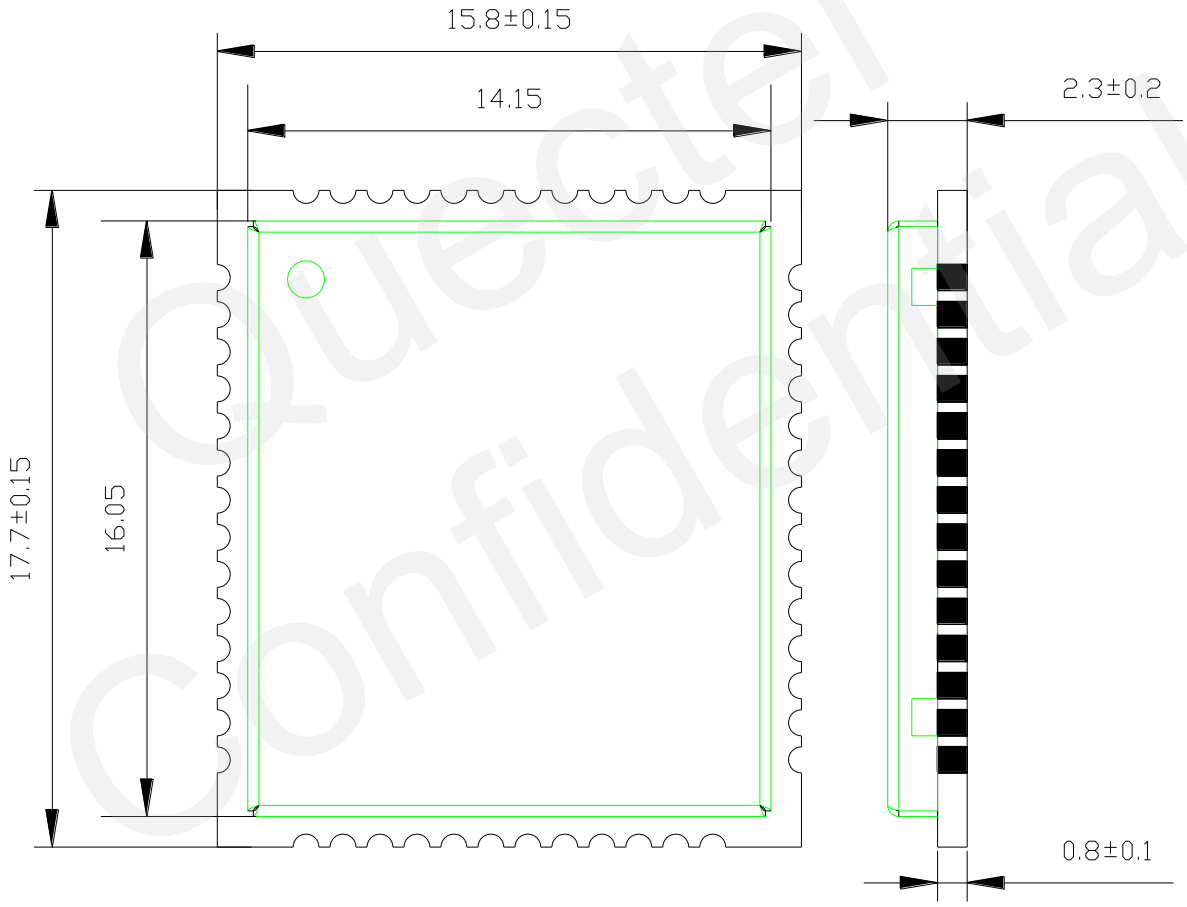

Figure 41: Top and Side Dimensions of M66-DS-OpenCPU (Unit: mm)

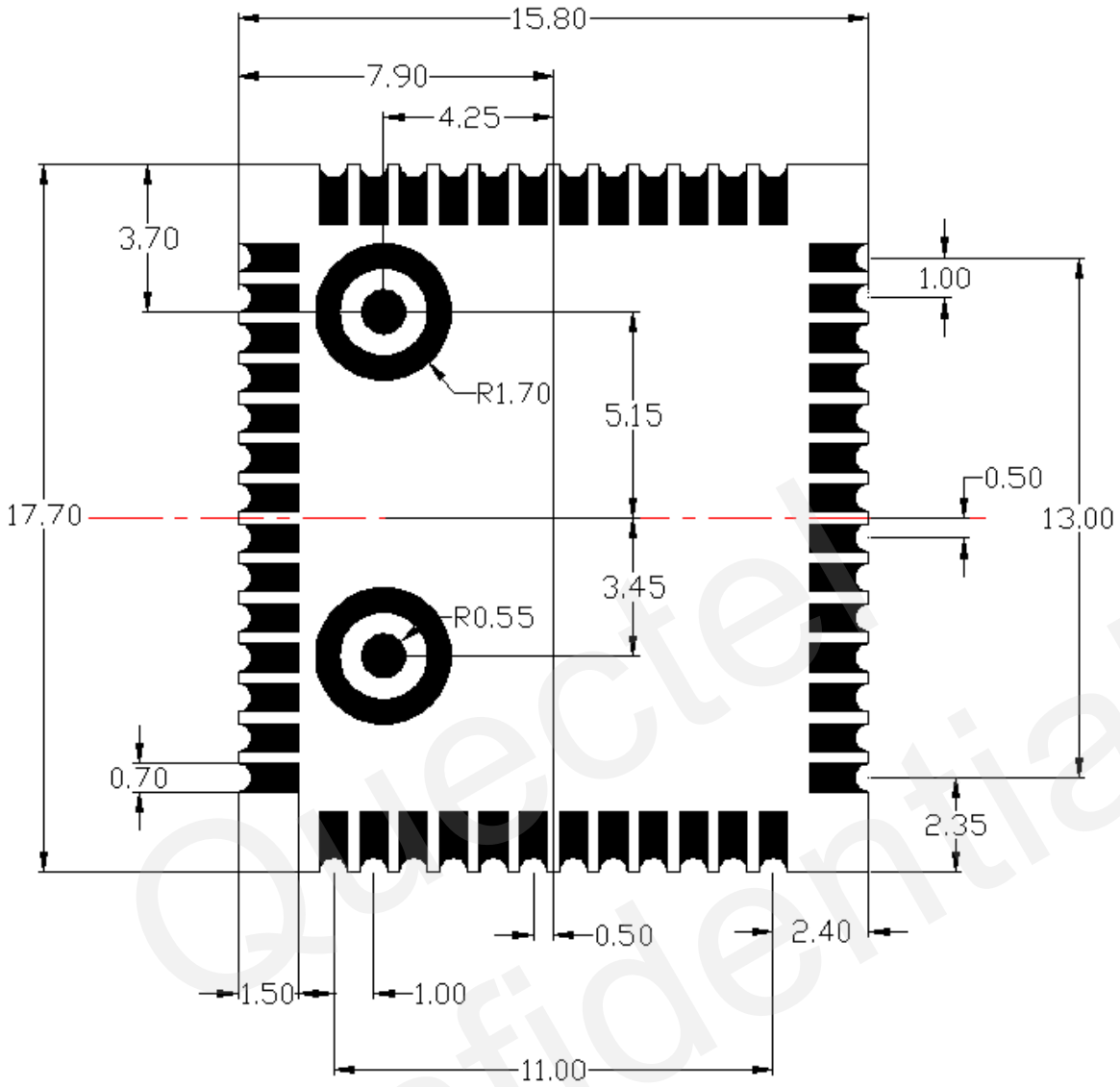

Figure 42: Bottom Dimensions of M66-DS-OpenCPU (Unit: mm)

6.2. Recommended Footprint

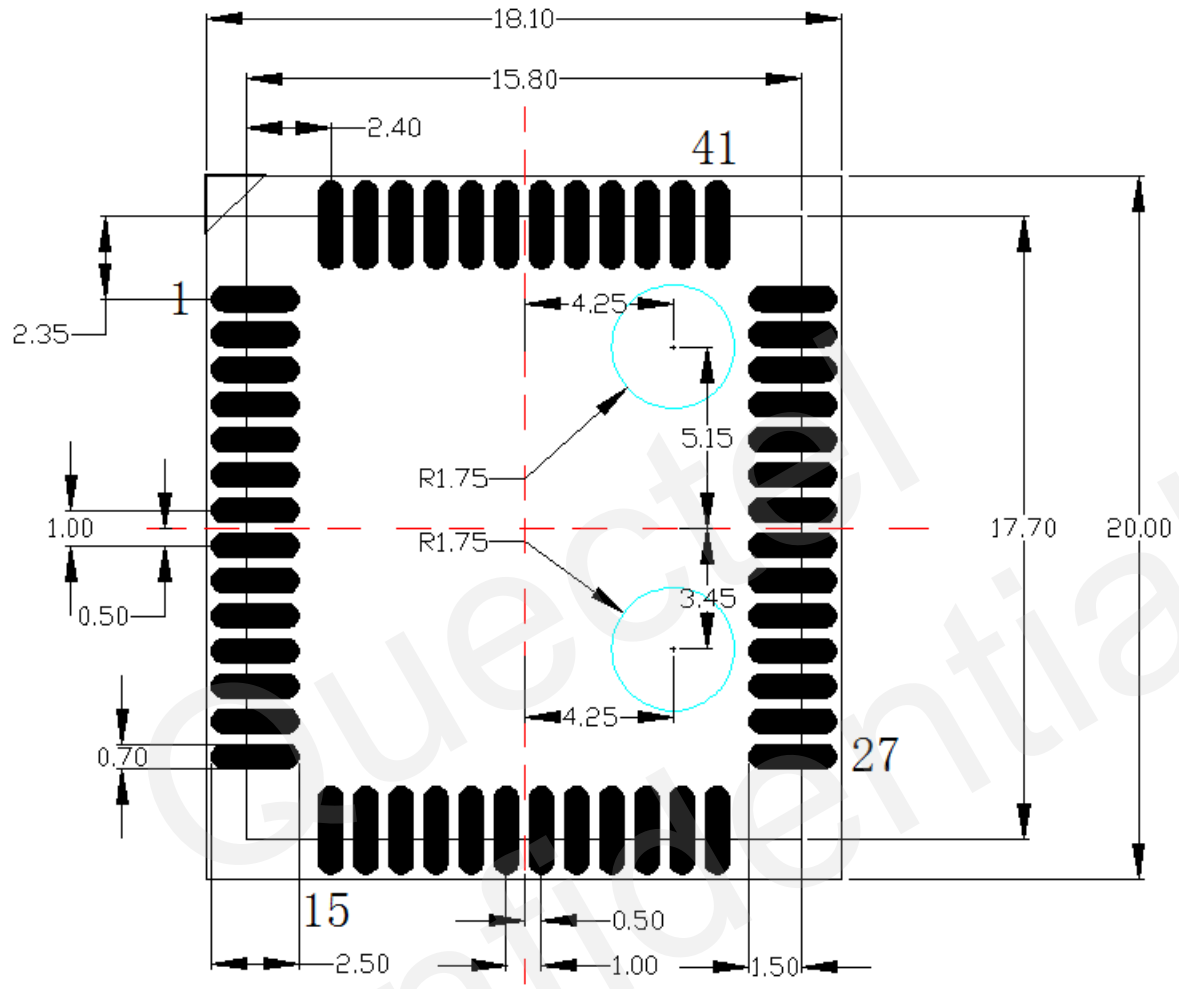

Figure 43: Recommended Footprint (Unit: mm)

NOTES

1. The module should be kept about 3mm away from other components in the host PCB.
2. The circular test points with a radius of 1.75mm in the above recommended footprint should be treated as keepout areas. ("keepout" means do not pour copper on the mother board).

6.3. Top and Bottom View of the Module

Figure 44: Top View of the Module

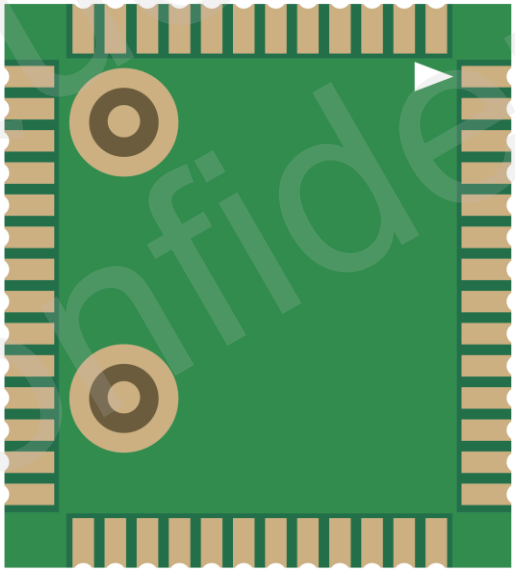

Figure 45: Bottom View of the Module

NOTE

These are design effect drawings of M66-DS-OpenCPU module. For more accurate pictures, please refer to the module that you get from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

M66-DS-OpenCPU module is stored in a vacuum-sealed bag. The storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC and <90%RH.

2. After the vacuum-sealed bag is opened, devices that need to be mounted directly must be:

- Mounted within 72 hours at the factory environment of ≤30ºC and <60% RH.
- Stored at <10% RH.

3. Devices require baking before mounting, if any circumstance below occurs.

- When the ambient temperature is 23ºC±5ºC, humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
- Device mounting cannot be finished within 72 hours when the ambient temperature is <30ºC and the humidity is <60%.
- Stored at >10% RH.

4. If baking is required, devices should be baked for 48 hours at 125ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (125ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

7.2. Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil at the hole of the module pads should be 0.2 mm for M66-DS-OpenCPU. For more details, please refer to the ***document [13]***

It is suggested that the peak reflow temperature is from 235 to 245ºC (for SnAg3.0Cu0.5 alloy). The absolute maximum reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below.

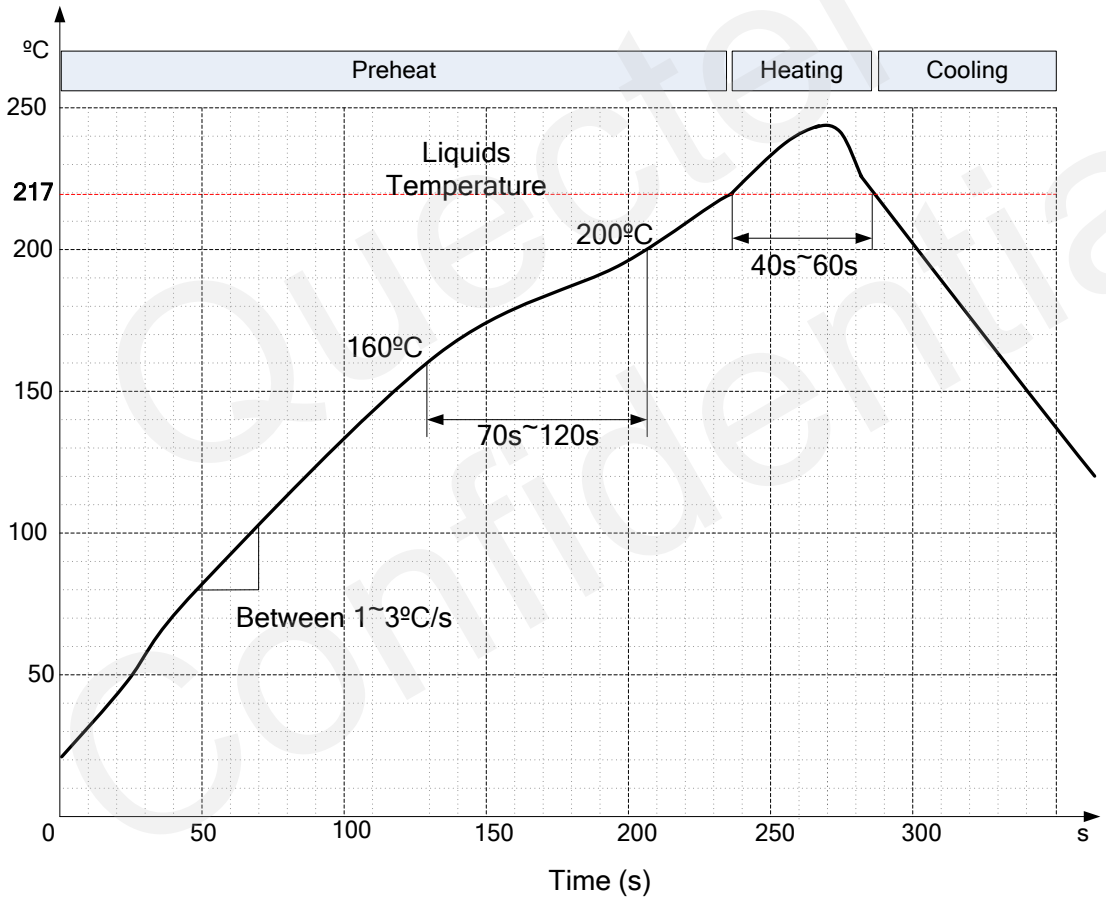

Figure 46: Reflow Soldering Thermal Profile

7.3. Packaging

M66-DS-OpenCPU module is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

7.3.1. Tape and Reel Packaging

The reel is 330mm in diameter and each reel contains 250 modules.

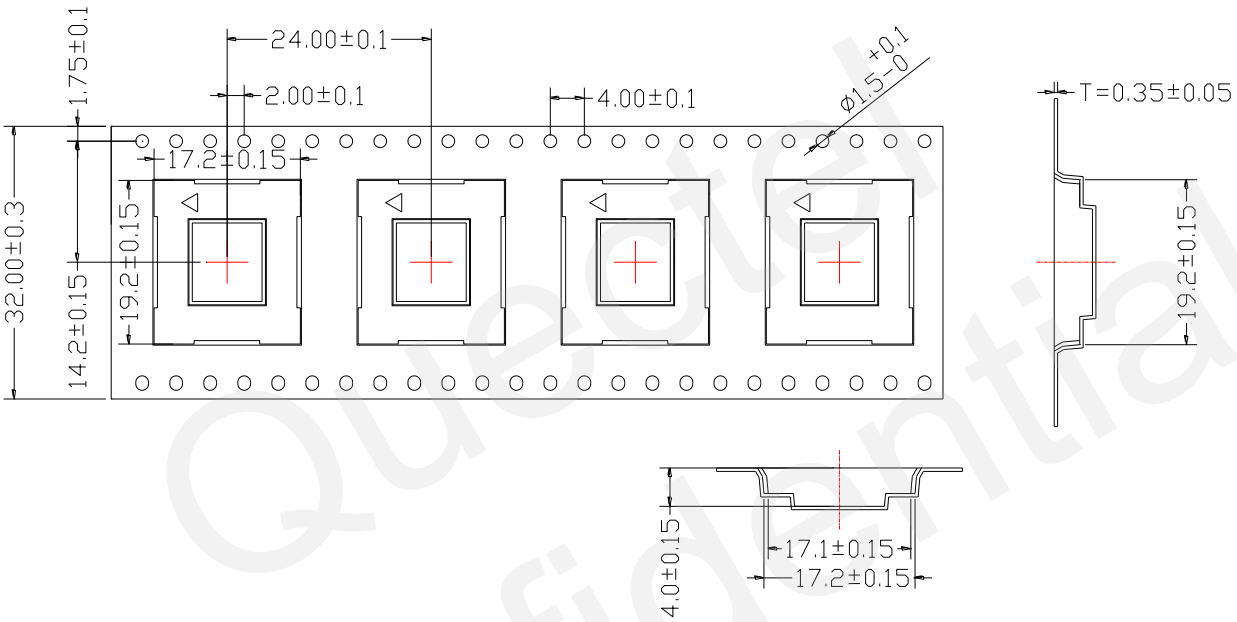

Figure 47: Tape Dimensions

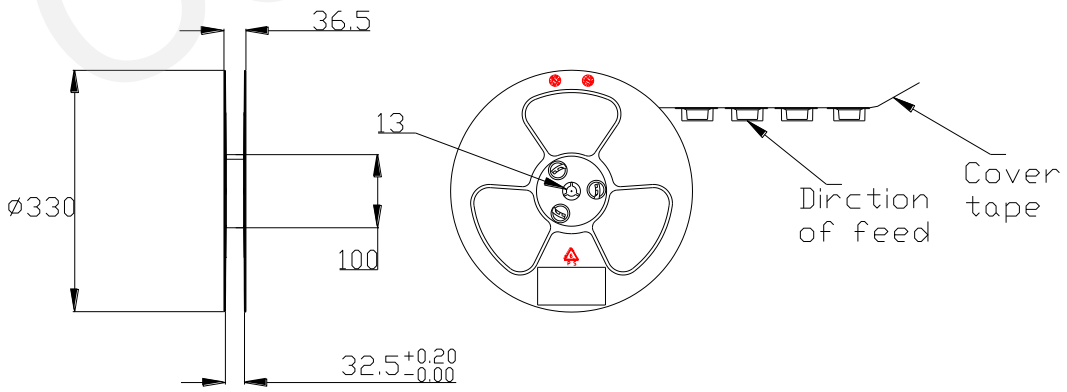

Figure 48: Reel Dimensions

8 Appendix A References

Table 42: Related Documents

SN	Document Name	Remark
[1]	Quectel_M66-DS_AT_Commands_Manual	AT commands manual for M66-DS
[2]	ITU-T Draft new recommendation V.25ter	Serial asynchronous automatic dialing and control
[3]	GSM 07.07	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[4]	GSM 07.10	Support GSM 07.10 multiplexing protocol
[5]	GSM 07.05	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[6]	GSM 11.14	Digital cellular telecommunications (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity module – Mobile Equipment (SIM – ME) interface
[7]	GSM 11.11	Digital cellular telecommunications (Phase 2+); Specification of the Subscriber Identity module – Mobile Equipment (SIM – ME) interface
[8]	GSM 03.38	Digital cellular telecommunications (Phase 2+); Alphabets and language-specific information
[9]	GSM 11.10	Digital cellular telecommunications (Phase 2); Mobile Station (MS) conformance specification; Part 1: Conformance specification
[10]	Quectel_GSM_UART_Application_Note	UART port application note
[11]	Quectel_GSM_EVB_User_Guide	GSM EVB user guide
[12]	Quectel_OpenCPU_User_Guide	Software design reference for OpenCPU
[13]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide

[14]	Quectel_GSM_Module_Digital_IO_Application_Note	GSM Module Digital IO application note

Table 43: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
ARP	Antenna Reference Point
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
BOM	Bill Of Material
BTS	Base Transceiver Station
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital-to-Analog Converter
DRX	Discontinuous Reception
DSP	Digital Signal Processor
DCE	Data Communications Equipment (typically module)
DTE	Data Terminal Equipment (typically computer, external controller)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge

ETS	European Telecommunication Standard
FCC	Federal Communications Commission (U.S.)
FDMA	Frequency Division Multiple Access
FR	Full Rate
FTP	File Transfer Protocol
GMSK	Gaussian Minimum Shift Keying
GPRS	General Packet Radio Service
GPI	General Purpose Input
GPO	General Purpose Output
GSM	Global System for Mobile Communications
HTTP	Hyper Text Transport Protocol
HO	High output
HR	Half Rate
I/O	Input/Output
L/H	Low/High
NTP	Network Time Protocol
PU/PD	Pull up/Pull down
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
Inorm	Normal Current
kbps	Kilo Bits Per Second
LED	Light Emitting Diode
Li-Ion	Lithium-Ion
MO	Mobile Originated

MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Switched Broadcast Control Channel
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RTC	Real Time Clock
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TCP/UDP	Transmission Control Protocol/ User Datagram Protocol
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
UART	Universal Asynchronous Receiver&Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio
$V_O$max	Maximum Output Voltage Value
$V_O$norm	Normal Output Voltage Value
$V_O$min	Minimum Output Voltage Value

V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}norm	Absolute Normal Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
Phonebook Abbreviations	
LD	SIM Last Dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT Calls (missed calls)
ON	SIM (or ME) Own Numbers (MSISDNs) list
RC	Mobile Equipment list of Received Calls
SM	SIM phonebook

9 Appendix B GPRS Coding Schemes

Four coding schemes are used in GPRS protocol. The differences between them are shown in the following table.

Table 44: Description of Different Coding Schemes

Scheme	Code Rate	USF	Pre-coded USF	Radio Block excl.USF and BCS	BCS	Tail	Coded Bits	Punctured Bits	Data Rate Kb/s
CS-1	1/2	3	3	181	40	4	456	0	9.05
CS-2	2/3	3	6	268	16	4	588	132	13.4
CS-3	3/4	3	6	312	16	4	676	220	15.6
CS-4	1	3	12	428	16	-	456	-	21.4

Radio block structure of CS-1, CS-2 and CS-3 is shown as the figure below.

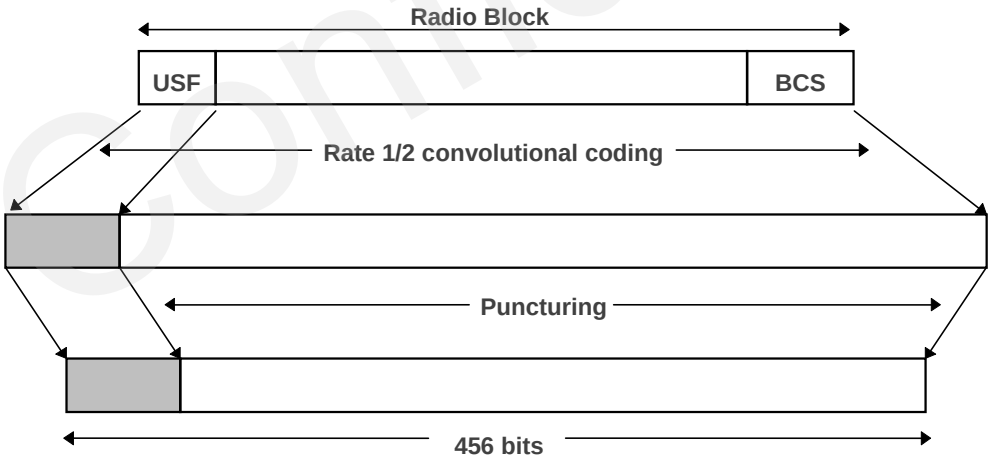

Figure 49: Radio Block Structure of CS-1, CS-2 and CS-3

Radio block structure of CS-4 is shown as the following figure.

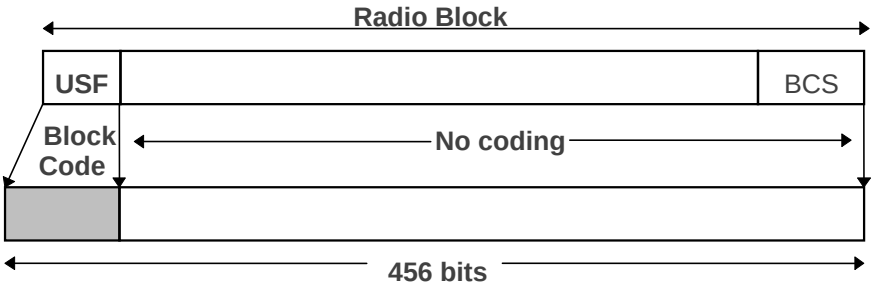

Figure 50: Radio Block Structure of CS-4

10 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications. The description of different multi-slot classes is shown in the following table.

Table 45: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5