M66-OpenCPU

Hardware Design

GSM/GPRS Module Series

Rev. M66-OpenCPU_Hardware_Design_V1.1

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About the Document

History

Revision	Date	Author	Description
1.0	2014-11-14	Felix YIN	Initial
1.1	2016-07-08	King MA	1. Modified the configuration and timing of PCM Interface 2. Added Chapter 3.9 SD Card Interface 3. Updated the description of Temperature Range

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1 Introduction

This document defines the M66-OpenCPU module and describes its hardware interface which are connected with the customer application and the air interface.

This document can help customer quickly understand module interface specifications, electrical and mechanical details. Associated with application notes and user guide, customer can use M66-OpenCPU module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating M66-OpenCPU module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel and to incorporate these guidelines into all manuals supplied with the product. If not so, Quectel does not take on any liability for customer failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobie while driving (even with a handsfree kit) cause distraction and can lead to an accident. You must comply with laws and regulations restrcting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers a Fight Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals or clinics or other health care facilities. These requests are desinged to prevent possible interference with sentitive medical equipment.
	Cellular terminals or mobiles operate over radio frequency signal and cellular network and cannot be guaranteed to connect in all conditions, for example no mobile fee or an invalid SIM card. While you are in this condition and need emergent help, Please Remember using emergency call. In order to make or receive call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is ON , it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potencially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potencially exposive atmospheres including fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Product Concept

2.1. General Description

OpenCPU is a method that the module acts as the main processor. With the developing communication technology and changing market, more and more customers have realized the advantages of OpenCPU solution. Especially, the advantage of reducing the product cost effectively is greatly valued by customers. With the help of OpenCPU solution, development flow for wireless application and hardware design will be simplified. The main features for OpenCPU solution are as below:

1. Reduce the product development period.
2. Simplify the circuit design and reduce the cost.
3. Decrease the product's size.
4. Decrease the power consumption.
5. Upgraded via OpenCPU FOTA.
6. Improve the performance-to-price ratio and enhance the competitive strength.

M66-OpenCPU module adopts the baseband processor with ARM7EJ-S™ core whose frequency can reach to 260MHz.

M66-OpenCPU is a Quad-band GSM/GPRS engine that works at frequencies of GSM850MHz, EGSM900MHz, DCS1800MHz and PCS1900MHz. The M66-OpenCPU module features GPRS multi-slot class 12 and supports the GPRS coding schemes CS-1, CS-2, CS-3 and CS-4. For more details about GPRS multi-slot classes and coding schemes, please refer to ***Appendix B*** and ***Appendix C***.

M66-OpenCPU is a SMD-type module with LCC package and a tiny profile of 15.8mm × 17.7mm × 2.3mm. Furthermore, M66-OpenCPU possesses abundant hardware interfaces and can be embedded into customer's application smoothly.

Designed with power saving technique, the current consumption of M66-OpenCPU module is as low as 1.3mA in Sleep Mode when DRX is 5.

M66-OpenCPU is integrated with internet service protocols, which are TCP/UDP, HTTP and FTP, etc. Customers can use these internet service protocols easily by calling the API functions.

M66-OpenCPU supports Bluetooth interface, it is fully compliant with Bluetooth specification 3.0.

The module fully complies with the RoHS directive of the European Union.

2.2. Key Features

The following table describes the detailed features of M66-OpenCPU module.

Table 1: Key Features

Feature	Implementation
Power Supply	Single supply voltage: 3.3V ~ 4.6V Typical supply voltage: 4V
Power Saving	Typical power consumption in SLEEP mode: 1.3 mA @DRX=5 1.2 mA @DRX=9
Frequency Bands	● Quad-band: GSM850, EGSM900, DCS1800, PCS1900. ● The module can search these frequency bands automatically ● The frequency bands can be set by **AT+QBAND** command ● Compliant to GSM Phase 2/2+
GSM Class	Small MS
Transmitting Power	● Class 4 (2W) at GSM850 and EGSM900 ● Class 1 (1W) at DCS1800 and PCS1900
GPRS Connectivity	● GPRS multi-slot class 12 (default) ● GPRS multi-slot class 1~12 (configurable) ● GPRS mobile station class B
DATA GPRS	● GPRS data downlink transfer: max. 85.6kbps ● GPRS data uplink transfer: max. 85.6kbps ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Support the protocols PAP (Password Authentication Protocol) ● Internet service protocols TCP/UDP, FTP, HTTP, NTP, PING ● Support Unstructured Supplementary Service Data (USSD)
Temperature Range	● Operation temperature range: -35°C ~ +75°C [1)] ● Extended temperature range: -40°C ~ +85°C [2)]
Bluetooth	● Support Bluetooth specification 3.0 ● Output Power: Class 1 (Typical 7.5dBm)
SMS	● Text and PDU mode ● SMS storage: SIM card ● MT MO
SIM Interface	Support SIM card: 1.8V, 3.0V
Audio Features	Speech codec modes: ● Half Rate (ETS 06.20)

	● Full Rate (ETS 06.10) ● Enhanced Full Rate (ETS 06.50/06.60/06.80) ● Adaptive Multi-Rate (AMR) ● Echo Suppression ● Noise Reduction
UART Interfaces	UART Port: ● Seven lines on UART port interface ● Used for AT command, GPRS data ● Multiplexing function Debug Port: ● Two lines on debug port interface DBG_TXD and DBG_RXD ● Debug Port only used for firmware debugging Auxiliary Port: ● Used for AT command
Phonebook Management	Support phonebook types: SM, ME, ON, MC, RC, DC, LD, LA
SIM Application Toolkit	Support SAT class 3, GSM 11.14 Release 99
Real Time Clock	Supported
Physical Characteristics	Size: 15.8±0.15 × 17.7±0.15 × 2.3±0.2mm Weight: Approx. 1.3g
Firmware Upgrade	● Via UART Port ● Via OpenCPU FOTA
Antenna Interface	Connected to antenna pad with 50 Ohm impedance control

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction; there are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP compliant again.

Table 2: Coding Schemes and Maximum Net Data Rates over Air Interface

Coding Scheme	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	9.05kbps	18.1kbps	36.2kbps
CS-2	13.4kbps	26.8kbps	53.6kbps

CS-3	15.6kbps	31.2kbps	62.4kbps
CS-4	21.4kbps	42.8kbps	85.6kbps

2.3. Functional Diagram

The following figure shows a block diagram of M66-OpenCPU and illustrates the major functional parts.

- Memory
- Radio frequency part
- Power management
- The peripheral interface
  —Power supply
  —Turn-on/off interface
  —UART interface
  —Audio interface
—PCM interface
—SPI interface
—I2C interface
  —SIM interface
  —SD interface
  —ADC interface
  —RF interface
  —BT interface

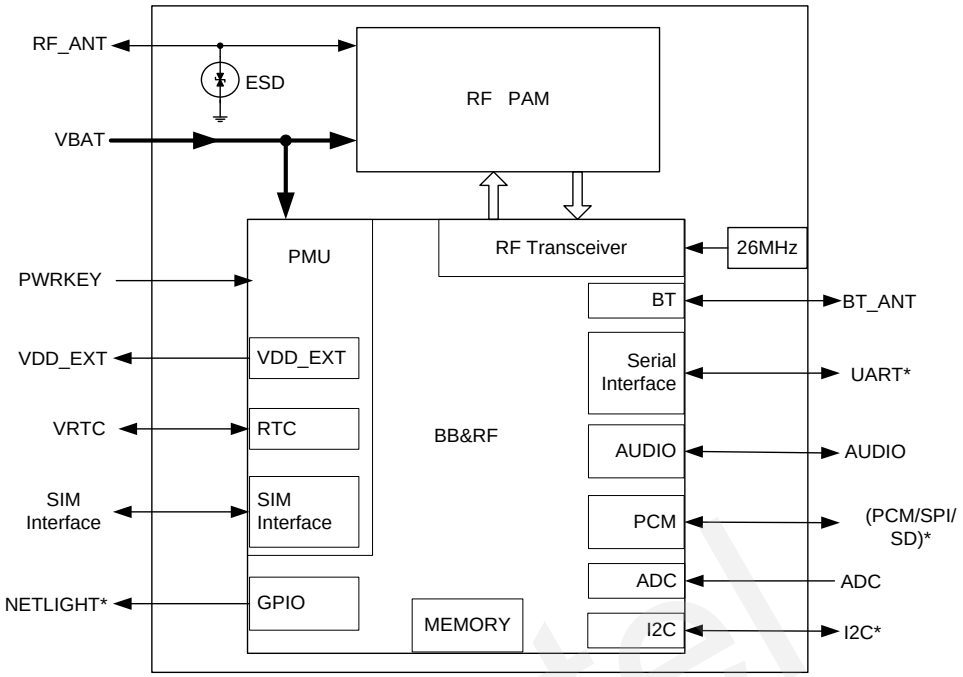

Figure 1: Module Functional Diagram

NOTE

About alternate functions of the interfaces marked with "*", please refer to ***Table 5***.

2.4. Pin Assignment

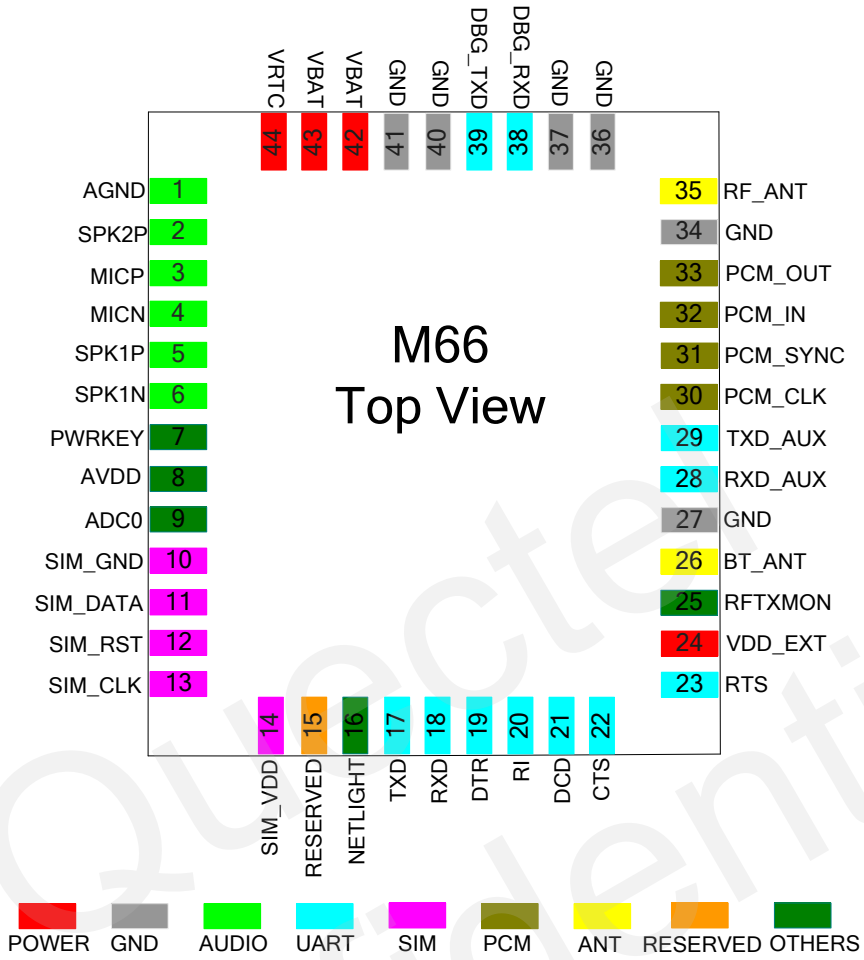

Figure 2: Pin Assignment

NOTE

Keep all reserved pins open.

Table 3: IO Parameters Definition

Type	Description
IO	Bidirectional input/output
DI	Digital input
DO	Digital output

PI	Power input
PO	Power output
AI	Analog input
AO	Analog output

Table 4: Pin Description

Power Supply					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42,43	PI	Main power supply of module: VBAT=3.3V~4.6V	$V_I$max=4.6V $V_I$min=3.3V $V_I$norm=4.0V	Make sure that supply sufficient current in a transmitting burst typically rises to 1.6A.
VRTC	44	IO	Power supply for RTC when VBAT is not supplied for the system. Charging for backup battery or golden capacitor when the VBAT is applied.	$V_I$max=3.3V $V_I$min=1.5V $V_I$norm=2.8V $V_O$max=3V $V_O$min=2V $V_O$norm=2.8V $I_O$max=2mA Iin≈10uA	If unused, keep this pin open.
VDD_EXT	24	PO	Supply 2.8V voltage for external circuit.	$V_O$max=2.9V $V_O$min=2.7V $V_O$norm=2.8V $I_O$max=20mA	1. If unused, keep this pin open. 2. Recommend to add a 2.2~4.7uF bypass capacitor, when using this pin for power supply.
GND	27,34 36,37 40,41		Ground		
Turn On/off					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Power on/off key. PWRKEY should be pulled down for a	V_{IL}max= 0.1×VBAT	

			moment to turn on or turn off the system.	V_{IH}min= 0.6×VBAT V_{IH}max=3.1V	
Audio Interface					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MICP MICN	3, 4	AI	Positive and negative voice input	Refer to Section 3.7	If unused, keep these pins open.
SPK1P SPK1N	5, 6	AO	Channel 1 positive and negative voice output		If unused, keep these pins open. Support both voice and ringtone output.
SPK2P	2	AO	Channel 2 voice output		
AGND	1		Analog ground. Separate ground connection for external audio circuits.		If unused, keep this pin open.
Network Status Indicator					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NETLIGHT	16	DO	Network status indication	V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	If unused, keep this pin open.
UART Port					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TXD	17	DO	Transmit data	V_{IL}min=0V V_{IL}max= 0.25×VDD_EXT V_{IH}min= 0.75×VDD_EXT V_{IH}max= VDD_EXT+0.2 V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	If only use TXD, RXD and GND to communicate, recommended connecting RTS to GND via 0R resistor and keeping other pins open.
RXD	18	DI	Receive data		
DTR	19	DI	Data terminal ready		
RI	20	DO	Ring indication		
DCD	21	DO	Data carrier detection		
CTS	22	DO	Clear to send		
RTS	23	DI	Request to send		
Debug Port					
PIN	**PIN**	**I/O**	**Description**	**DC Characteristics**	**Comment**

Name	No.				
DBG_TXD	39	DO	Transmit data	Same as above	If unused, keep these pins open.
DBG_RXD	38	DI	Receive data		
Auxiliary Port					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TXD_AUX	29	DO	Transmit data	Same as above	If unused, keep these pins open.
RXD_AUX	28	DI	Receive data		
SIM Interface					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SIM_VDD	14	PO	Power supply for SIM card	The voltage can be selected by software automatically. Either 1.8V or 3.0V.	All signals of SIM interface should be protected against ESD with a TVS diode array. Maximum trace length is 200mm from the module pad to SIM card holder.
SIM_CLK	13	DO	SIM clock	V_{OL}max= 0.15×SIM_VDD V_{OH}min= 0.85×SIM_VDD	
SIM_DATA	11	IO	SIM data	V_{IL}max= 0.25×SIM_VDD V_{IH}min= 0.75×SIM_VDD V_{OL}max= 0.15×SIM_VDD V_{OH}min= 0.85×SIM_VDD	
SIM_RST	12	DO	SIM reset	V_{OL}max= 0.15×SIM_VDD V_{OH}min= 0.85×SIM_VDD	
SIM_GND	10		SIM ground		
ADC					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

AVDD	8	PO	Reference voltage of ADC circuit	$V_O$max=2.9V $V_O$min=2.7V $V_O$norm=2.8V	If unused, keep this pin open.
ADC0	9	AI	General purpose analog to digital converter.	Voltage range: 0V to 2.8V	If unused, keep this pin open.
PCM					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	30	DO	PCM clock	V_{IL}min= 0V V_{IL}max= 0.25×VDD_EXT V_{IH}min= 0.75×VDD_EXT V_{IH}max= VDD_EXT+0.2 V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	
PCM_SYNC	31	DO	PCM frame synchronization		
PCM_IN	32	DI	PCM data input		
PCM_OUT	33	DO	PCM data output		
Antenna Interface					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RF_ANT	35	IO	GSM antenna pad	Impedance of 50Ω	
BT_ANT	26	IO	BT antenna pad	Impedance of 50Ω	
Transmitting Signal Indication					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	
RFTXMON	25	DO	Transmission signal indication	V_{OH}min= 0.85×VDD_EXT V_{OL}max= 0.15×VDD_EXT	
Other Interface					
PIN Name	**PIN No.**	**I/O**	**Description**	**DC Characteristics**	
RESERVED	15				Keep these pins open.

Table 5: Multiplexed Functions

PIN Name	PIN No.	Mode1 (Default)	Mode 2	Mode 3	Mode 4
NETLIGHT	16	NETLIGHT	GPIO	PWM	
DTR	19	DTR	GPIO	EINT	SIM_PRESENCE
RI	20	RI	GPIO	I2C_SCL	
DCD	21	DCD	GPIO	I2C_SDA	
CTS	22	CTS	GPIO		
RTS	23	RTS	GPIO		
RXD_AUX	28	RXD_AUX	GPIO		
TXD_AUX	29	TXD_AUX	GPIO		
PCM_CLK	30	PCM_CLK	GPIO	SPI_CS	
PCM_ SYNC	31	PCM_SYNC	GPIO	SPI_MISO	SD_DATA
PCM_IN	32	PCM_IN	GPIO	SPI_CLK	SD_CMD
PCM_OUT	33	PCM_OUT	GPIO	SPI_MOSI	SD_CLK

2.5. Operating Modes

The table below briefly summarizes the various operating modes.

Table 6: Overview of Operating Modes

Mode	Function	
Normal Operation	GSM/GPRS Sleep	After enabling sleep mode by calling **Ql_SleepEnable()**, the module will automatically enter into Sleep Mode when CPU is in idle state. In this case, the current consumption of module will reduce to the minimal level. During Sleep Mode, the module can still receive paging message and SMS from the network normally.
	GSM IDLE	Software is active. The module has registered to the GSM network, and the module is ready to send and receive GSM

		data.
	GSM TALK	GSM connection is ongoing. In this mode, the power consumption is decided by the configuration of Power Control Level (PCL), dynamic DTX control and the working RF band.
	GPRS IDLE	The module is not registered to GPRS network. The module is not reachable through GPRS channel.
	GPRS STANDBY	The module is registered to GPRS network, but no GPRS PDP context is active. The SGSN knows the Routing Area where the module is located at.
	GPRS READY	The PDP context is active, but no data transfer is ongoing. The module is ready to receive or send GPRS data. The SGSN knows the cell where the module is located at.
	GPRS DATA	There is GPRS data in transfer. In this mode, power consumption is decided by the PCL, working RF band and GPRS multi-slot configuration.
POWER DOWN	Normal shutdown calling **Ql_PowerDown()** or using the PWRKEY pin. The power management ASIC disconnects the power supply from the base band part of the module, and only the power supply for the RTC is remained. Software is not active. The UART interfaces are not accessible. Operating voltage (connected to VBAT) remains applied.	
Minimum Functionality Mode (without removing power supply)	**AT+CFUN** command can set the module to a minimum functionality mode without removing the power supply. In this case, the RF part of the module will not work or the SIM card will not be accessible, or both RF part and SIM card will be disabled, but the UART port is still accessible. The power consumption in this case is very low.	

2.6. Flash Memory Allocation

A 32M-bit flash memory is used in the module. The flash memory allocation is shown as below.

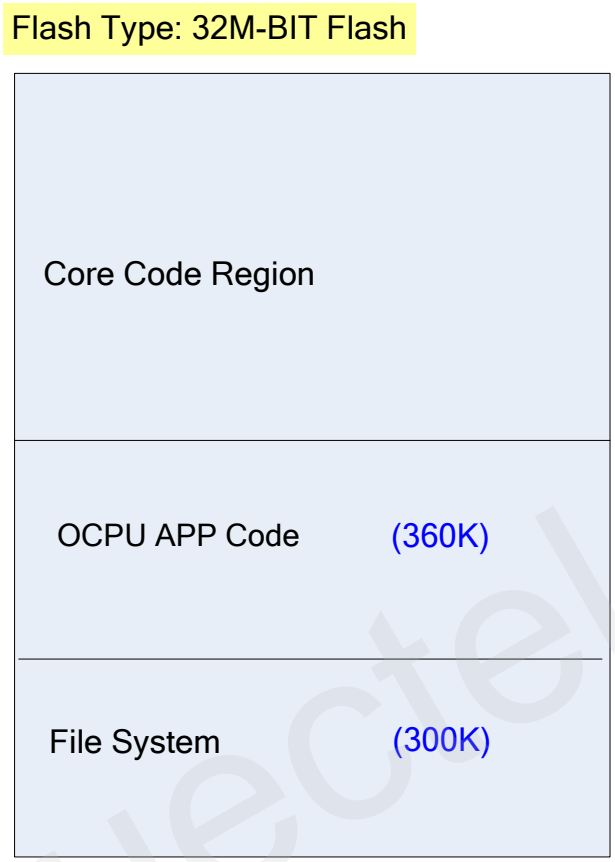

Figure 3: FLASH Memory Allocation

M66-OpenCPU module allocates 360KB space for customer's code and 300KB file system space which is used to store the data (e.g. system configuration file, temporary data, image, multimedia file, and so on) related to file operation.

- RAM

M66-OpenCPU reserves 100KB RAM space for the embedded application and provides about 500KB dynamic memory at most.

3 Application Interface

3.1. General Description

The module adopts LCC package and has 44 pins. The following chapters provide detailed descriptions about these pins.

- Power supply
- Power on/down
- Power saving
- RTC
- Serial interfaces
- Audio interfaces
- SIM card interface
- SD card interface
- PCM interface
- SPI and I2C interface
- ADC
- External interrupts
- PWM
- GPIO
- RF transmitting signal indication

3.2. Power Supply

3.2.1. Power Features of Module

The power supply is an important point during designing GSM terminals. Due to the 577us radio burst emission in GSM every 4.615ms, power supply must be able to deliver high current peaks in a burst period. During these peaks, drops on the supply voltage must not exceed minimum working voltage of module.

For the M66-OpenCPU module, the max current consumption could reach to 1.6A during a transmit burst. It will cause a large voltage drop on the VBAT. In order to ensure stable operation of the module, it is recommended that the max voltage drop for VBAT during the transmit burst does not exceed 400mV.

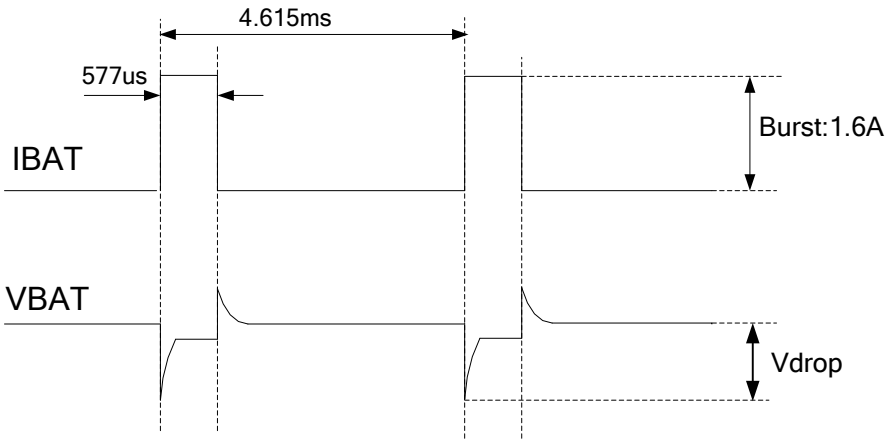

Figure 4: Voltage Ripple during Transmitting

3.2.2. Decrease Supply Voltage Drop

The power supply range of the module is 3.3V to 4.6V. Make sure that the input voltage will never drop below 3.3V even in a transmitting burst. If the power voltage drops below 3.3V, the module could turn off automatically. For better power performance, it is recommended to place a 100uF tantalum capacitor with low ESR (ESR=0.7Ω) and a ceramic capacitor (100nF~1uF) near the VBAT pin. In order to improve the RF interference, other low capacitance capacitors should be placed close to VBAT pin. The reference circuit is illustrated in Figure 5.

The VBAT route should be wide enough to ensure that there is not too much voltage drop occurring during transmit burst. The width of trace should be no less than 2mm and the principle of the VBAT route is the longer route, the wider trace.

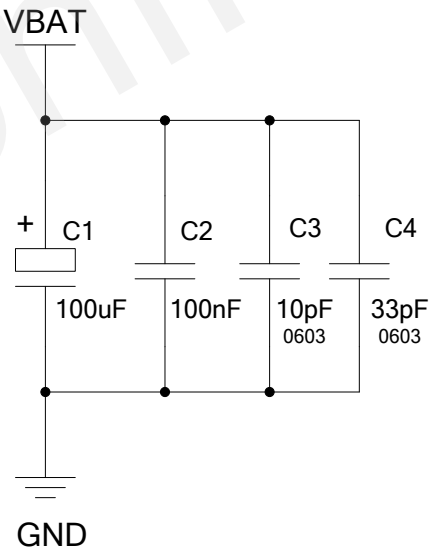

Figure 5: Reference Circuit for the VBAT Input

3.2.3. Reference Design for Power Supply

The power design for the module is very important, since the performance of power supply for the module largely depends on the power source. The power supply is capable of providing the sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested to use a LDO as module's power supply. If there is a big voltage difference between the input source and the desired output (VBAT), a switcher power converter is recommended to be used as a power supply.

The following figure shows a reference design for +5V input power source. The designed output for the power supply is 4.0V and the maximum load current is 3A. In addition, in order to get a stable output voltage, a zener diode is placed close to the pins of VBAT. As to the zener diode, it is suggested to use a zener diode whose reverse zener voltage is 5.1V and dissipation power is more than 1 Watt.

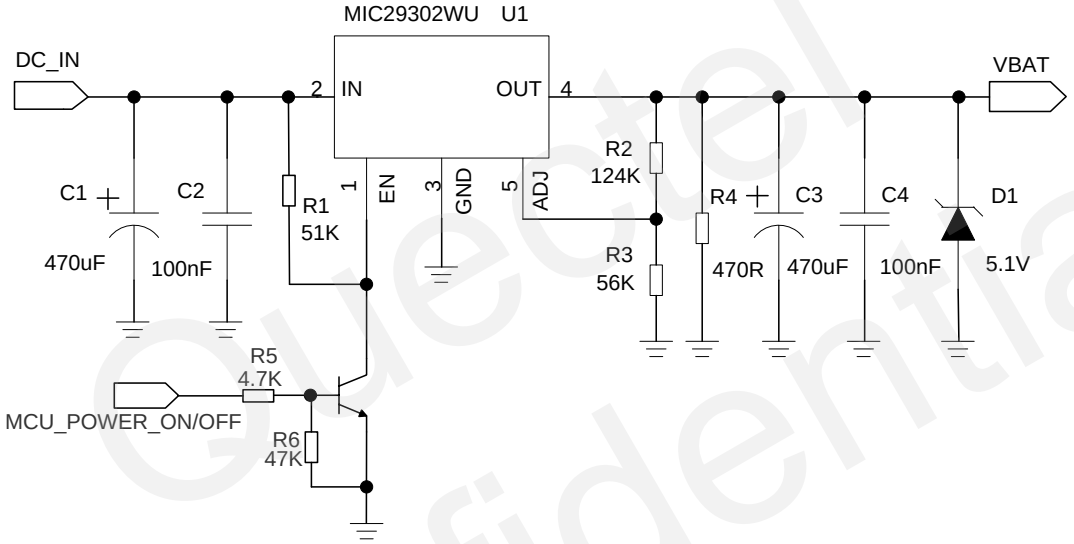

Figure 6: Reference Circuit for Power Supply

NOTE

It is suggested to control the module's main power supply (VBAT) via LDO enable pin to restart the module when the module has become abnormal. Power switch circuit like P-channel MOSFET switch circuit can also be used to control VBAT.

3.2.4. Monitor Power Supply

The module can monitor the supply voltage by using **AT+CBC** command or calling **RIL_GetPowerSupply()**. Your application program can start a timer and periodically use **AT+CBC** command or call **RIL_GetPowerSupply()** to check the power supply.

For more information about the software design, please refer to the ***document [12]***.

3.3. Power on and down Scenarios

3.3.1. Power on

The module can be turned on by driving the pin PWRKEY to a low level voltage. An open collector driver circuit is suggested to control the PWRKEY. A simple reference circuit is illustrated as below.

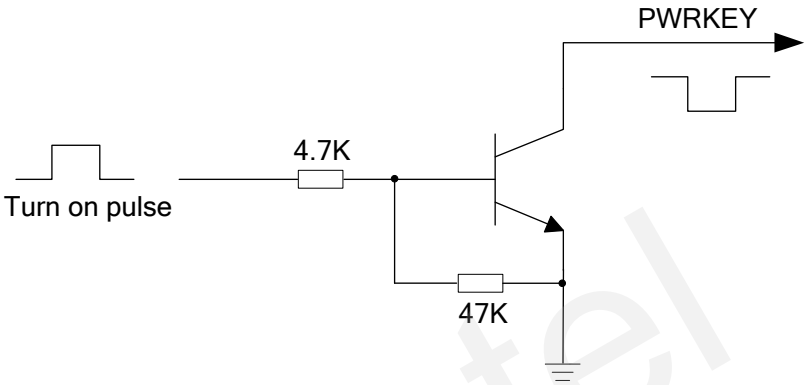

Figure 7: Turn on the Module with an Open-collector Driver

The other way to control the PWRKEY is through a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. For the best performance, the TVS component must be placed nearby the button. When pressing the key, electrostatic strike may generate from finger. A reference circuit is shown in the following figure.

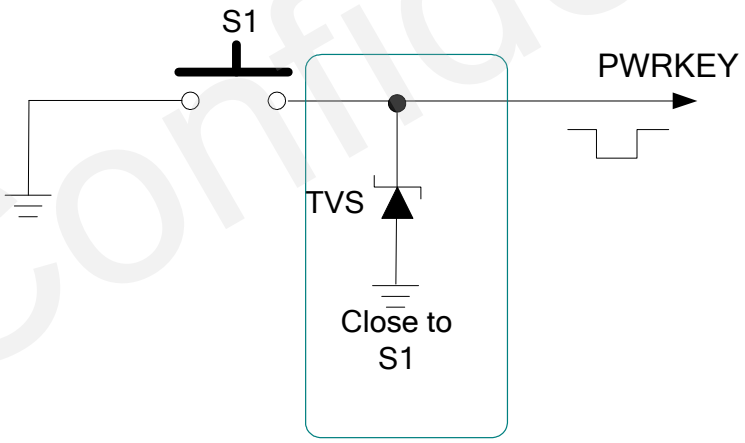

Figure 8: Turn on the Module with a Button

The turn-on timing is illustrated as the following figure.

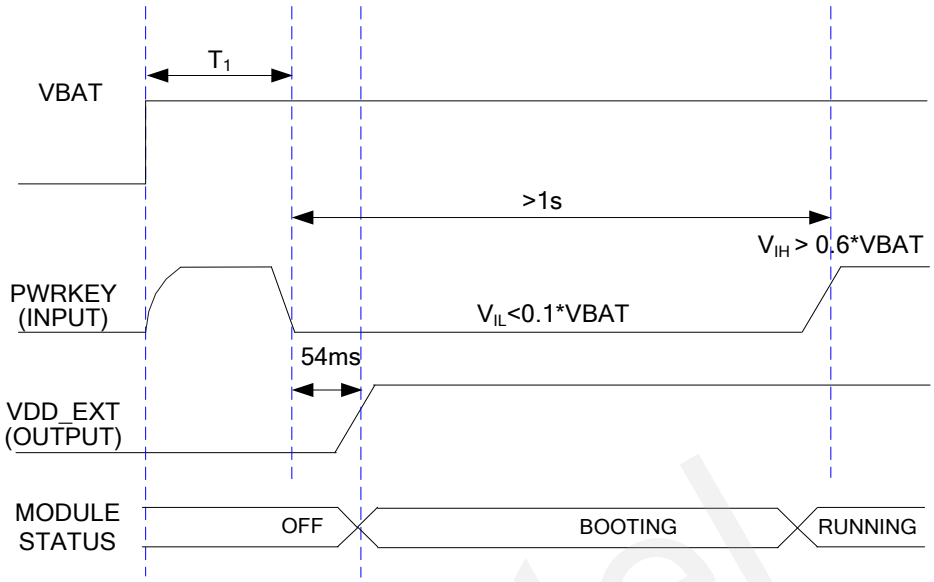

Figure 9: Turn-on Timing

NOTES

1. Make sure that VBAT voltage is stable before pulling down PWRKEY pin. The time of T1 is recommended as 100ms.
2. Set PWRKEY low for at least 1 second to turn on the system. If the PWRKEY is set as low consistently, the module can also be turned on, but in this case, PWRKEY cannot be used to turn off the module.

3.3.2. Power down

The following methods can be used to turn off the module.

- Normal power down procedure: Turn off module using the PWRKEY pin
- Normal power down procedure: Turn off module by executing command **AT+QPOWD** or calling API **Ql_PowerDown()**
- under-voltage automatic shutdown: Take effect when under-voltage is detected.

3.3.2.1. Power down Module Using the PWRKEY Pin

Set the PWRKEY pin low for a certain time and then the module will be turned off. During turn-off, the module will log off from the network and save important data. As logout network time is related to the local mobile network, it is recommended to delay about 12 seconds before disconnecting the power supply or restarting the module.

After the PWRKEY pin is set to low, the module will be powered down by calling API function. For more information about software design, please refer to *the* ***document [12]***.

After turn-off, the module enters into POWER DOWN Mode. The turn-off timing is shown as below.

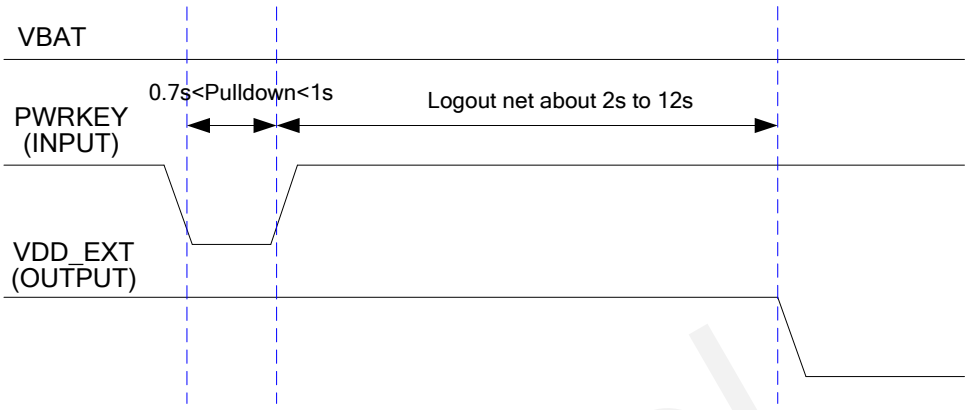

Figure 10: Turn-off Timing

NOTE

If the PWRKEY pin is used to turn off the module, it cannot be set to low consistently. Otherwise, the module will restart after being turned off.

3.3.2.2. Power down Module Using the API Function

Module can achieve normal turn-off through calling an API function **Ql_PowerDown()**.

For detailed information about the software design, please refer to the ***document [12]***.

3.3.2.3. Under-voltage Automatic Shutdown

Under-voltage will cause the module to turn off. The module will constantly monitor the voltage applied on the VBAT. If any circumstance shown below occurs, the module will notify customer's application through Callback functions.

- VBAT voltage is ≤ 3.5V: under-voltage warning.
- VBAT voltage is <3.3V: under-voltage turn-off.

For detailed information about the software design, please refer to the ***document [12]***.

3.3.3. Recommended Turn-on Structure for OpenCPU System

In order to ensure the stability of OpenCPU system, it is suggested to use a low-power MCU to monitor the status of the module. The MCU should possess several GPIOs and one ADC interface. The system structure is shown in the figure below. This structure possesses two advantages:

- When the VBAT voltage detected by ADC is too low, the MCU will turn off the module by controlling PWRKEY pin and switch off power supply by controlling the PMOS transistor.
- Normally, the module outputs periodic pulse to the MCU. If the MCU does not detect the pulse within the stipulated time, the MCU will switch off VBAT and then turn on the module again.

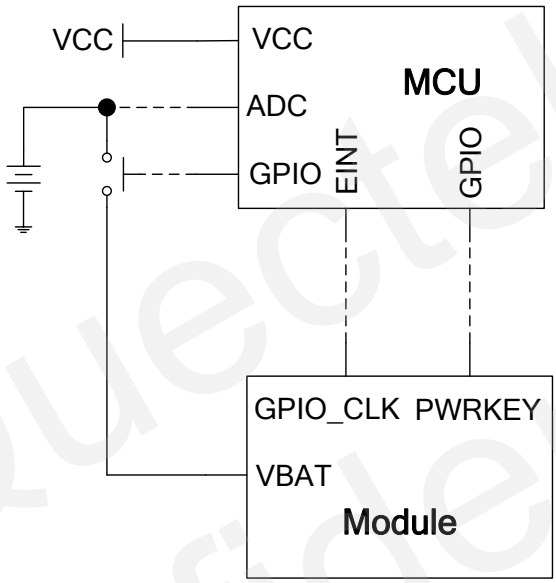

Figure 11: Recommended Turn-on Structure for OpenCPU System

Furthermore, a watchdog component can also be used to control the power of module. A watchdog component with timeout of 1.6s at least should be used, for instance, TI's TPS3823-33DBVR. One GPIO of module should be connected to the WDI pin of the watchdog and change the electrical level of the WDI pin timely. If timeout occurs, the watchdog will switch off the power of module. The sketch map for watchdog is shown as below.

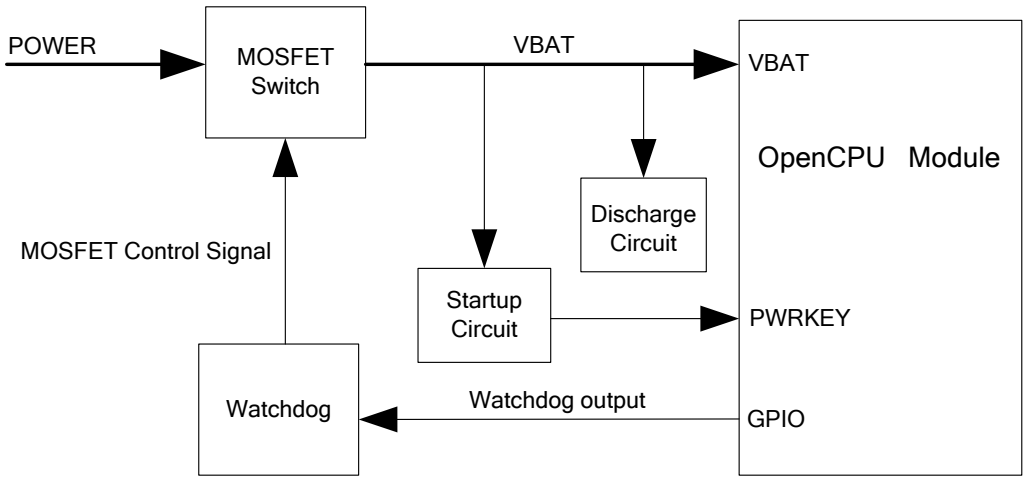

Figure 12: Sketch Map for Watchdog

NOTE

If the power of module is controlled by watchdog circuit, and the module is only powered by VRTC, when power is switched off the real time will have an error about 5 minutes a day.

3.4. Power Saving

Based on system requirements, there are two methods to drive the module to enter into low current consumption status. One is to use the API function to make the module enter into Minimum Functionality Mode, the other is to use the API function to make the module enter into Sleep Mode.

3.4.1. Minimum Functionality Mode

M66-OpenCPU module reduces its functionality to minimum level in order to minimize the current consumption in Minimum Functionality Mode. M66-OpenCPU module can enter into Minimum Functionality Mode through using **AT+CFUN=0** command. If the returned value is not equal to 1, the module can enter into Full Functionality Mode through using **AT+CFUN=1** command. For detailed information about software design, please refer to the ***document [12]***.

3.4.2. Sleep Mode

After entering into Sleep Mode, M66-OpenCPU module can still receive calls, SMS and GPRS data, but the serial interfaces do not work. The Sleep Mode is disabled by default. The module can enter into Sleep Mode when it is idle through calling the API function **Ql_SleepEnable()**.

When M66-OpenCPU module is in Sleep Mode, the following methods can wake it up.

- Incoming call
- SMS or MMS
- GPRS data
- External interrupts
- System timer timeout

The following methods can make the module exit from Sleep Mode.

- Call the API function **Ql_SleepDisable()** when the application program is executed.

For detailed information about software design, please refer to the ***document [12]***.

3.5. RTC

The RTC (Real Time Clock) function is supported. The RTC is designed to work with an internal power supply.

There are three kinds of designs for RTC backup power:

- **Use VBAT as the RTC power source**

When the module is turned off and the main power supply (VBAT) is remained, the real time clock is still active as the RTC core is supplied by VBAT. In this case, the VRTC pin can be kept floating.

- **Use VRTC as the RTC power source**

If the main power supply (VBAT) is removed after the module is turned off, a backup supply such as a coin-cell battery (rechargeable or non-chargeable) or a super-cap can be used to supply the VRTC pin to keep the real time clock active.

- **Use VBAT and VRTC as the RTC power source**

As only power the VRTC pin to keep the RTC will lead an error about 5 minutes a day, it is recommended to power VBAT and VRTC pin at the same time when RTC function is needed. The recommended supply for RTC core circuits are shown as below.

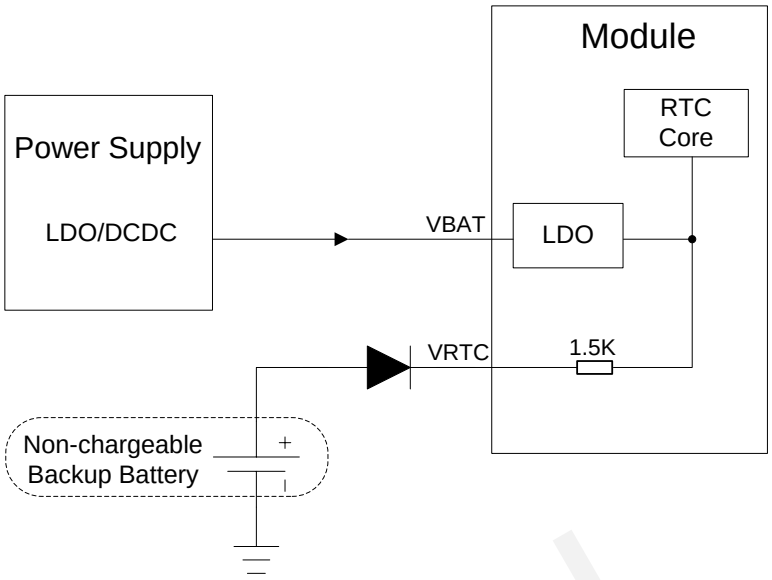

Figure 13: VRTC is Supplied by a Non-chargeable Battery

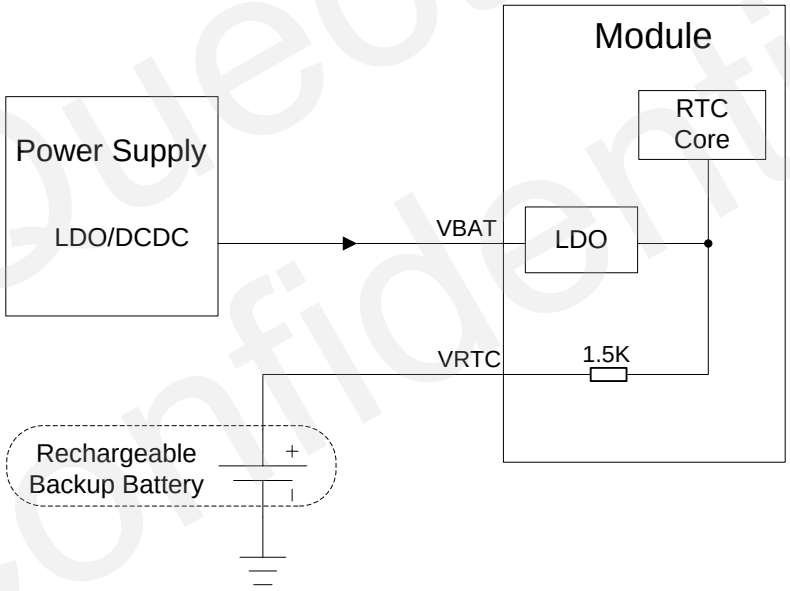

Figure 14: VRTC is Supplied by a Rechargeable Battery

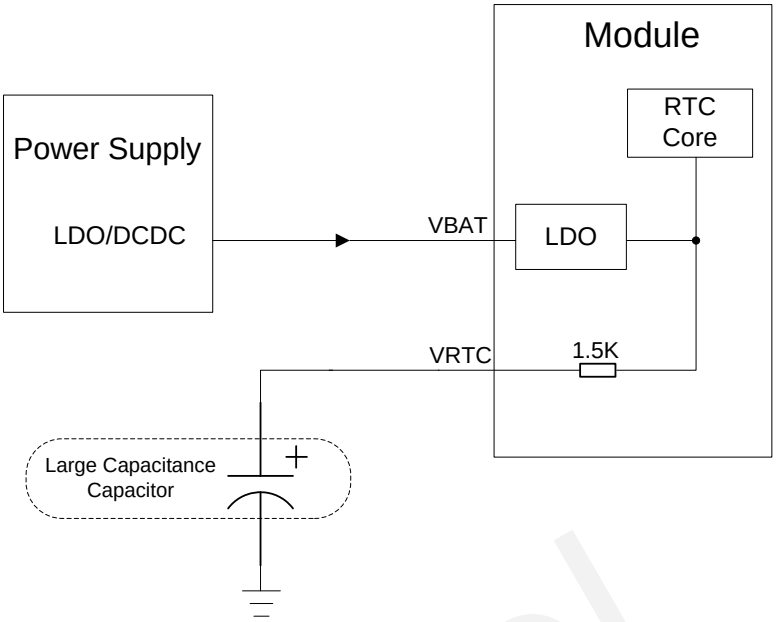

Figure 15: VRTC is Supplied by a Capacitor

A rechargeable or non-chargeable coin-cell battery can also be used here, for more information, please visit http://www.sii.co.jp/en/.

API functions related to RTC are shown as below:

- Get RTC time: **Ql_GetLocalTime()**
- Set RTC time: **Ql_SetLocalTime()**

For detailed information about software design, please refer to the ***document [12].***

NOTE

If want to keep an accurate real time, please keep the main power supply VBAT alive .

3.6. Serial Interfaces

The module provides three serial ports: UART Port, Debug Port and Auxiliary UART Port. The module is designed as a DCE (Data Communication Equipment), which should be used according to the traditional DCE-DTE (Data Terminal Equipment) connection. The module adopts fixed baudrate and its default baudrate is 115200.

The UART Port:

- TXD: Send data to RXD of DTE.
- RXD: Receive data from TXD of DTE.
- RTS: Request to send.
- CTS: Clear to send.
- DTR: DTE is ready and inform DCE (this pin can wake up the module).
- RI: Ring indication (when there is a call, SMS or URC output, the module will inform DTE with the RI pin.)
- DCD: Data carrier detection.

The Debug Port:

- DBG_TXD: Send data to the RXD of DTE
- DBG_RXD: Receive data from the TXD of DTE

The Auxiliary UART Port:

- TXD_AUX: Send data to the RXD of DTE
- RXD_AUX: Receive data from the TXD of DTE

The logic levels of these serial interfaces are described in the following table.

Table 7: Logic Levels of the UART Interface

Parameter	Min.	Max.	Unit
V_{IL}	0	0.25×VDD_EXT	V
V_{IH}	0.75×VDD_EXT	VDD_EXT +0.2	V
V_{OL}	0	0.15×VDD_EXT	V
V_{OH}	0.85×VDD_EXT	VDD_EXT	V

Table 8: Pin Definition of the UART Interfaces

Interface	Pin No.	Pin Name	Description
UART Port	17	TXD	Transmit data
	18	RXD	Receive data

	19	DTR	Data terminal ready
	20	RI	Ring indication
	21	DCD	Data carrier detection
	22	CTS	Clear to send
	23	RTS	Request to send
Debug Port	38	DBG_RXD	Receive data
	39	DBG_TXD	Transmit data
Auxiliary UART Port	28	RXD_AUX	Receive data
	29	TXD_AUX	Transmit data

NOTE

If DCD, RI, DTR, CTS and RTS are not used, they can be multiplexed as GPIOs. As to GPIO, please refer to Section ***3.14 GPIO***.

Functions and events related to serial interfaces are as below:

- **Ql_UART_Register**: register a callback for the specified serial port.
- **Ql_UART_Open**: open the specified serial port.
- **Ql_UART_Write**: send data to the specified serial port.
- **Ql_UART_Read**: read data from the specified serial port.
- **Ql_UART_SetDCBConfig**: set DCB of serial port.
- **EVENT_UART_READY_TO_READ**: read indication when data comes.

For detailed information about software design, please refer to the ***document [12].***

3.6.1. UART Port

3.6.1.1. The Features of UART Port.

- 8 data bits, no parity bit, one stop bit.
- Firmware upgrade and data communication.
- Supported baud rates are as below:
  300, 600, 2400, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800.
- The module adopts a fixed baud rate and its default baud rate is 115200.
- Support hardware flow control, but it is disabled by default.

NOTES

1. The API function **QI_UART_SetDCBConfig** can be used to set different baudrate.
2. The API function **QI_UART_Open** can be used to set hardware flow control.

3.6.1.2. Reference Design for UART Port

The reference design for UART Port is shown as below.

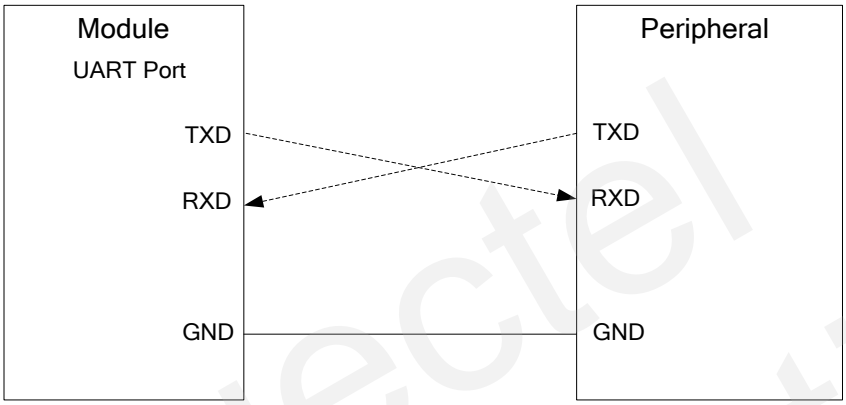

Figure 16: Reference Design for UART Port

3.6.1.3. Firmware Upgrade

The UART Port can be used to upgrade firmware. The PWRKEY pin must be pulled down before the firmware upgrade. The following cautions must be taken into account.

- VBAT voltage must be stable.
- PWRKEY pin must be set low

The following figure shows the reference design for firmware upgrade.

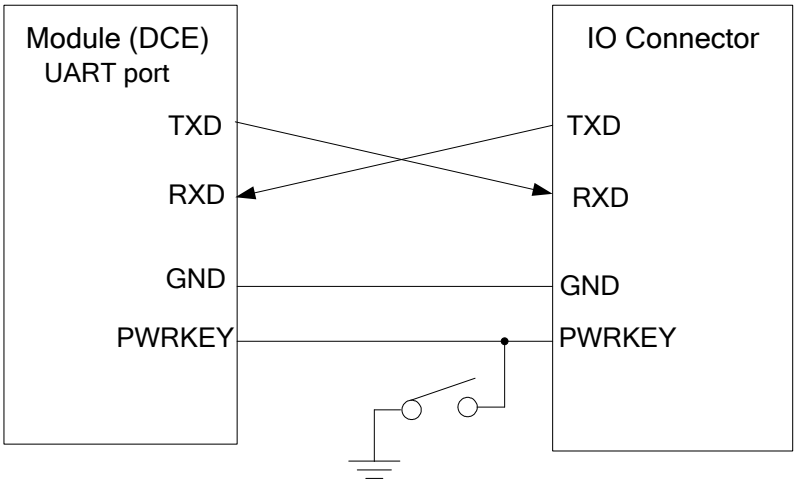

Figure 17: Reference Design for Firmware Upgrade

3.6.2. Debug Port

As to Debug Port, there are two working modes, Basic Mode and Advanced Mode, which can be switched through configuring APP software.

- Under Basic Mode, it can be used to execute software debug and it can also connect to a peripheral device. Furthermore, its default baud rate is 115200bps.
- Under Advanced Mode, it can only be used to execute software debug, capture the system's log with Cather tool and call **QI_Debug_Trace()** to output the application log. In this mode, its baud rate is 460800bps.

The reference design for Debug Port is shown as below.

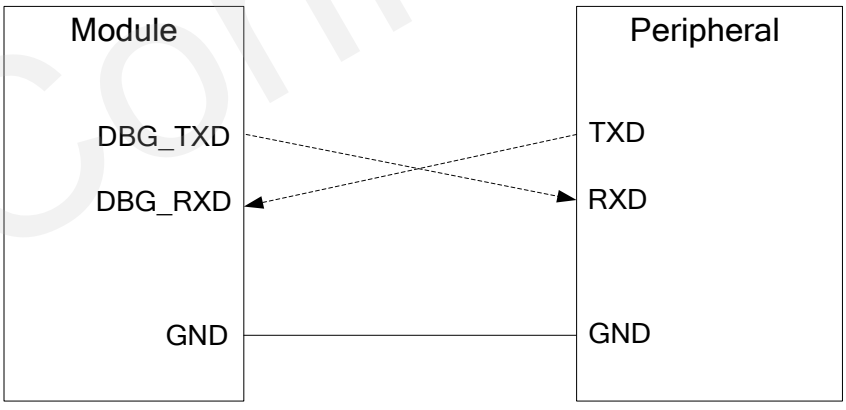

Figure 18: Reference Design for Debug Port

3.6.3. Auxiliary UART Port

Auxiliary UART Port:

- 8 data bits, no parity bit, one stop bit.
- Supported baud rates are as below:
  1200, 2400, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800.
- The default baud rate is 115200bps.

The reference design for Auxiliary UART Port is shown as below.

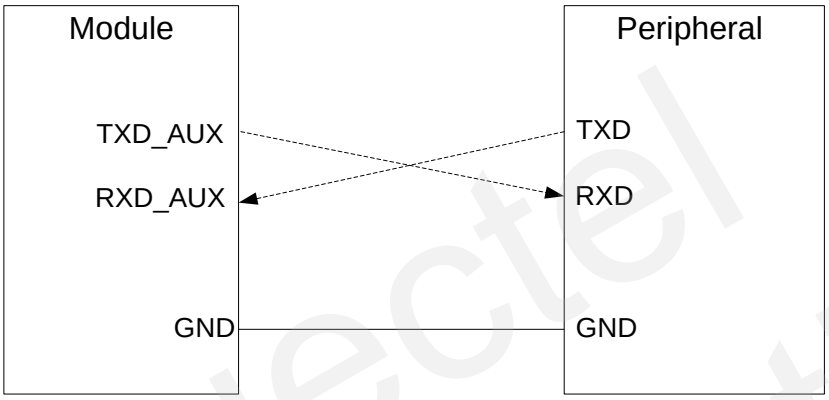

Figure 19: Reference Design for Auxiliary UART Port

3.6.4. UART Application

The reference design for 3.3V level match is shown as below. If the peripheral is a 3V system, please change the 5.6K resistor to 10K.

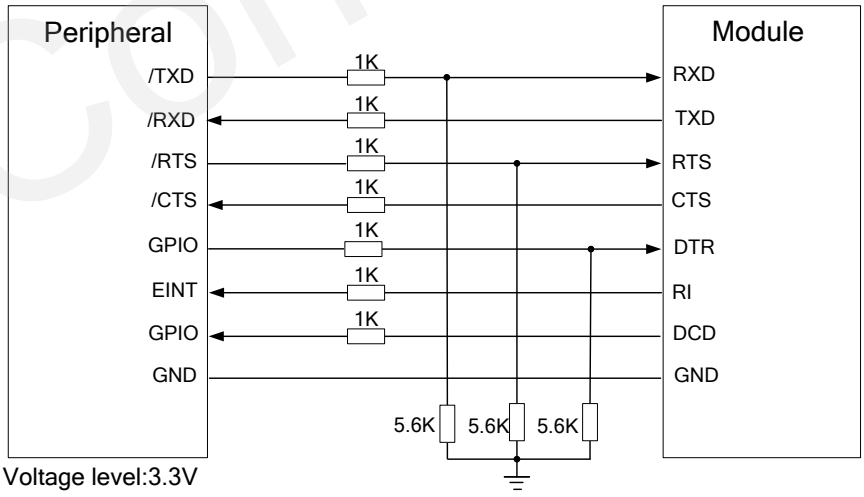

Figure 20: Level Match Design for 3.3V System

NOTE

It is highly recommended to add the resistor divider circuit on the UART signal lines when the host's level is 3V or 3.3V. For the higher voltage level system, a level shifter IC could be used between the host and the module. For more details about UART circuit design, please refer to ***document [14]***.

The following figure shows a sketch map between module and standard RS-232 interface. Since the electrical level of module is 2.8V, so a RS-232 level shifter must be used. Note that you should assure the IO voltage of level shifter which connects to module is 2.8V.

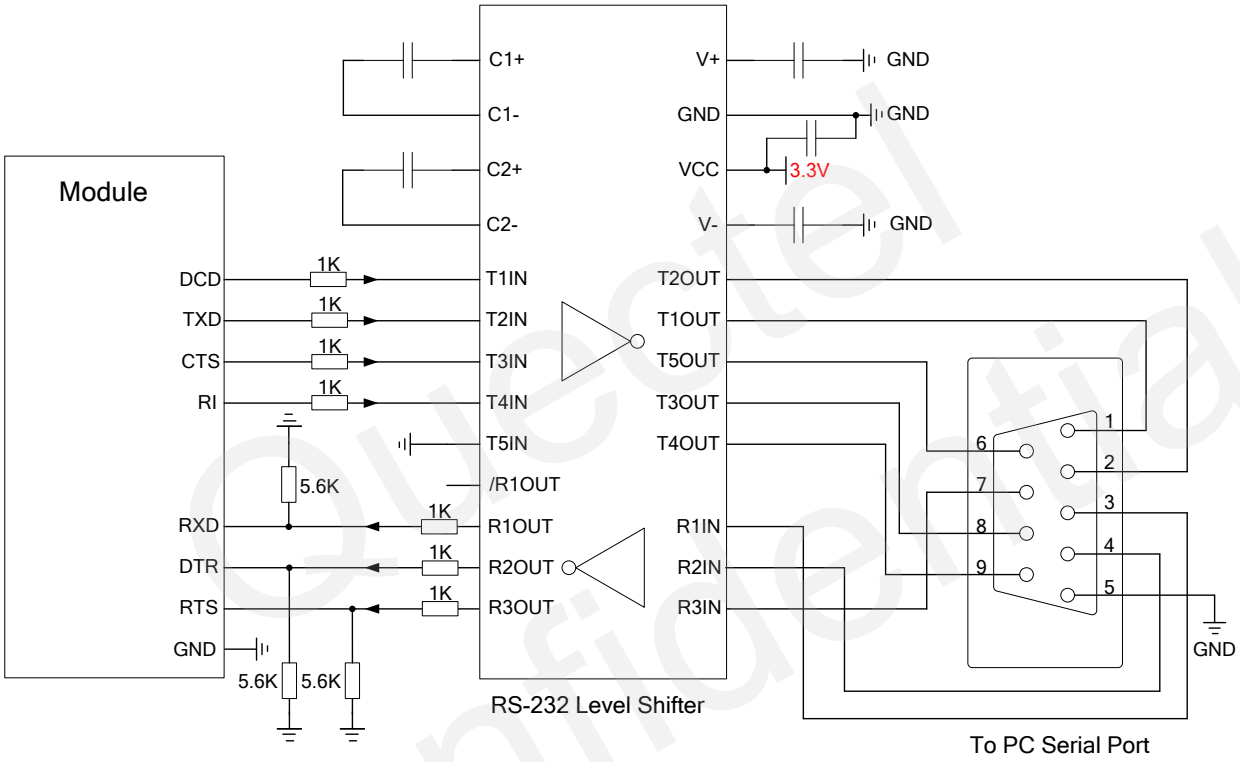

Figure 21: Sketch Map for RS-232 Interface Match

Please visit vendor web site to select correct IC, such as: http://www.maximintegrated.com and http://www.exar.com/.

3.7. Audio Interfaces

The module provides one analog audio input channel and two analog audio output channels.

Table 9: Pin Definition of Audio Interface

Interface	Name	Pin NO.	Description
AIN/AOUT1	MICP	3	Microphone positive input
	MICN	4	Microphone negative input
	SPK1P	5	Channel 1 Audio positive output
	SPK1N	6	Channel 1 Audio negative output
AIN/AOUT2	MICP	3	Microphone positive input
	MICN	4	Microphone negative input
	SPK2P	2	Channel 2 Audio positive output
	AGND	1	Form a pseudo-differential pair with SPK2P

Features about two audio interfaces are described as below:

- AIN are used for input of microphone or line. An electret microphone is usually used. AIN are differential input channels.
- AOUT1 is an output channel used for a receiver. This channel is typically used for a receiver. AOUT1 channel is a differential channel and it supports voice and ringtone output, and so on.
- AOUT2 is typically used for a headset. It is a single-ended and mono channel. SPK2P and AGND can form a pseudo differential pair and it supports voice and ringtone output, and so on.
- Select the audio channel with command **AT+QAUDCH**.
- Adjust the input gain of the microphone with command **AT+QMIC**.
- Adjust the output gain for receiver or speaker with command **AT+CLVL**.
- Configure the parameters of echo cancellation function with command **AT+QECHO**.
- Configure the side tone gain with command **AT+QSIDET**.

3.7.1. Decrease TDD Noise and Other Noise

It is suggested to use the electret microphone with built-in RF filtering capacitors (e.g. 10pF and 33pF). The 33pF capacitor is applied for filtering out 900MHz RF interference when the module is transmitting at EGSM900MHz. Without this capacitor, TDD noise could be heard. Moreover, the 10pF capacitor here is for filtering out 1800MHz RF interference. Since the resonant frequency point of a capacitor largely depends on the material and production technique, therefore, customers need to discuss with their capacitor vendor

to choose the most suitable capacitor for filtering out GSM850MHz, EGSM900MHz, DCS1800MHz and PCS1900MHz separately.

The RF interference in the audio channel during GSM transmitting period largely depends on the application design. In some cases, EGSM900 TDD noise is more severe, while in other cases, DCS1800 TDD noise is more obvious. Therefore, customers can select the suitable capacitors according to the test result. Sometimes, even RF filtering capacitor is not required.

The capacitor which is used for filtering out RF noise should be close to audio interfaces. Furthermore, the audio trace should be as short as possible.

In order to decrease radio or other signal interference, the RF antenna should be kept away from audio interface, and the RF trace should be away from the audio trace. In addition, the power trace should also be away from the audio trace.

Finally, the differential audio traces must be routed according to the differential signal layout rule.

3.7.2. Reference Design for AIN

AIN channel come with internal bias supply for external electret microphone. A reference circuit is shown in the following figure.

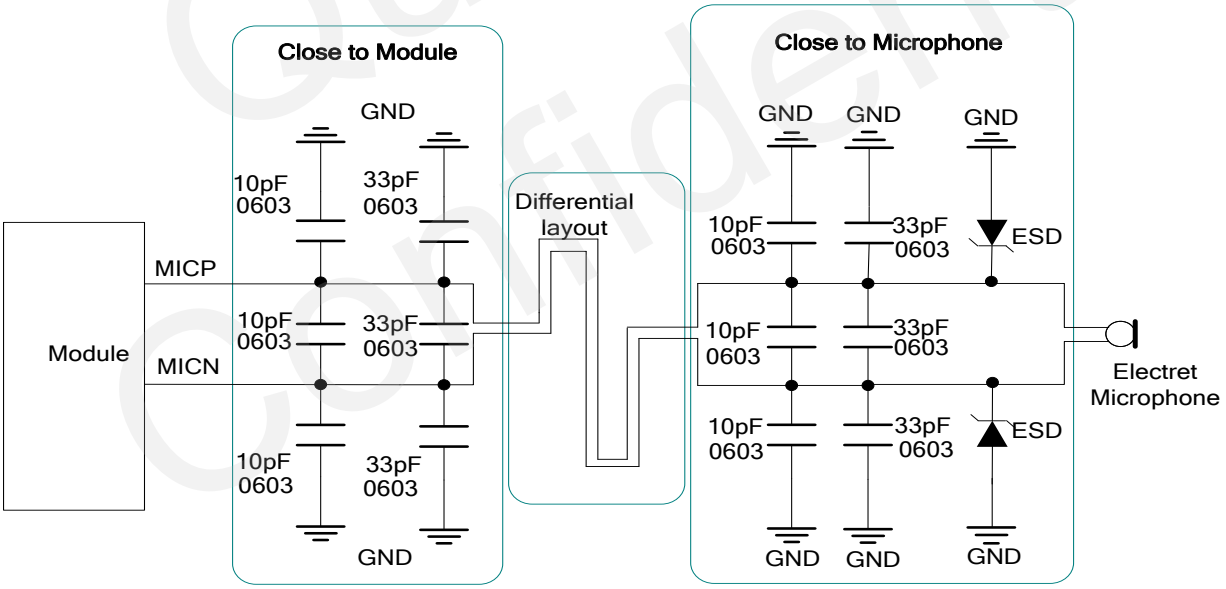

Figure 22: Reference Design for AIN

3.7.3. Reference Design for AOUT1 and AOUT2

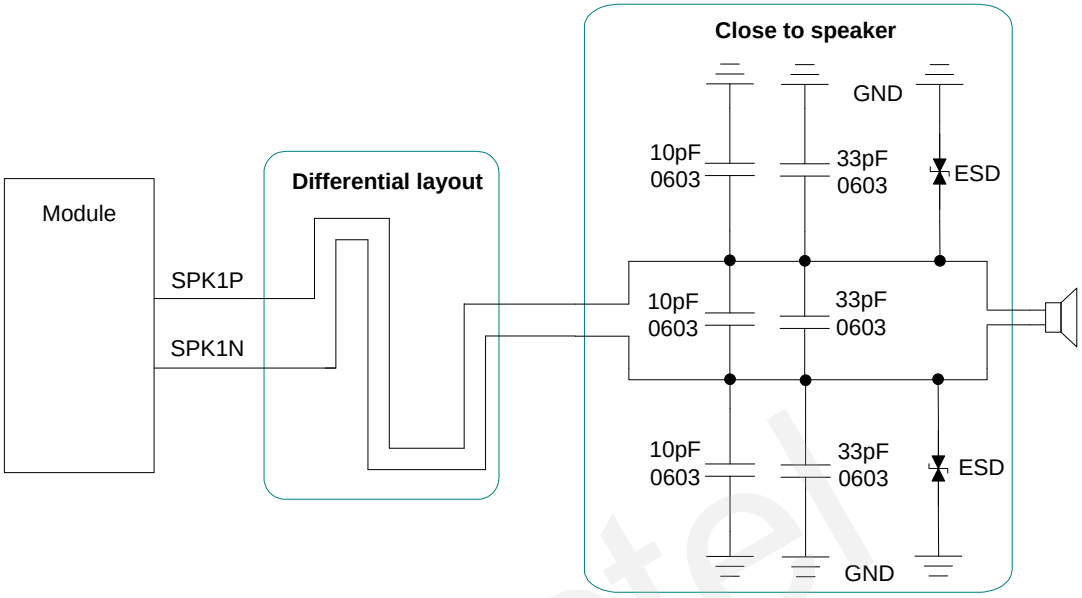

Figure 23: Reference Design for AOUT1

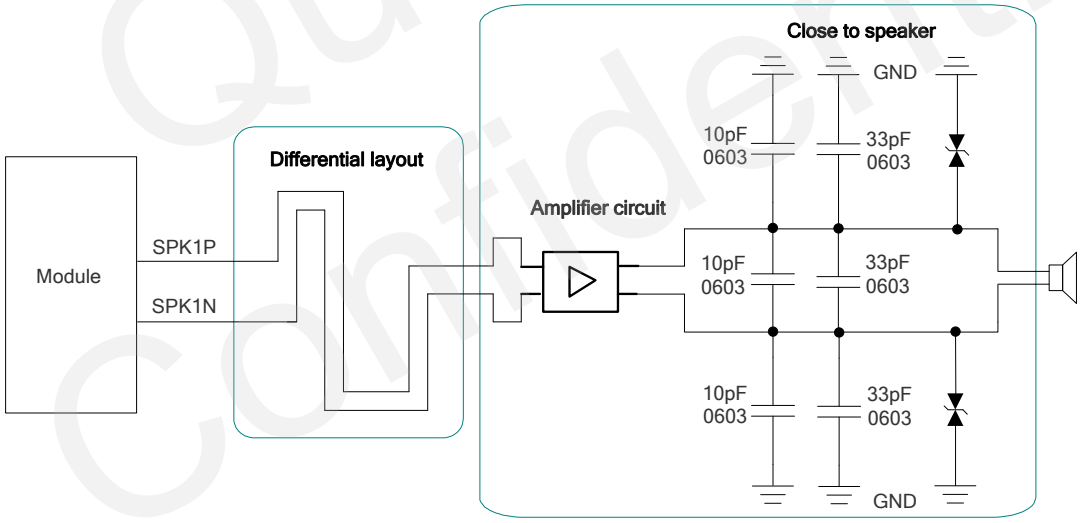

Figure 24: Reference Design with an Amplifier for AOUT1

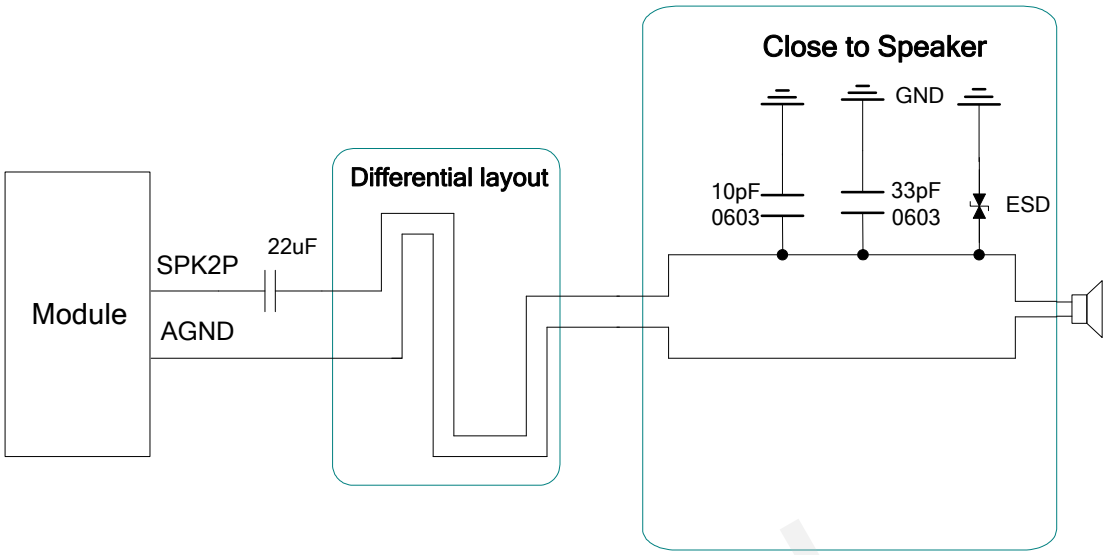

Figure 25: Reference Design for AOUT2

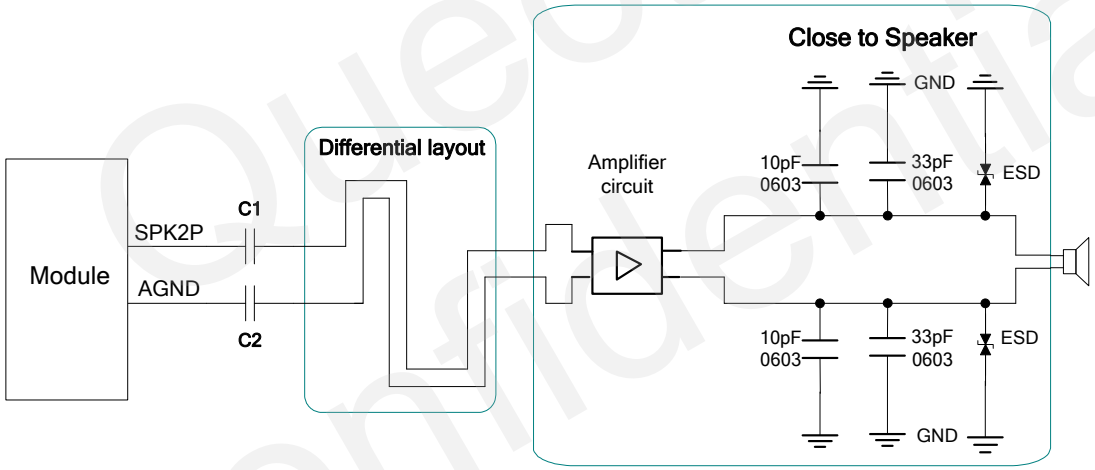

Figure 26: Reference Design with an Amplifier for AOUT2

The suitable differential audio amplifier can be chosen from the Texas Instrument's website (http://www.ti.com/). There are also other excellent audio amplifier vendors in the market.

NOTE

The value of C1 and C2 depends on the input impedance of the audio amplifier.

3.7.4. Reference Design for an Earphone

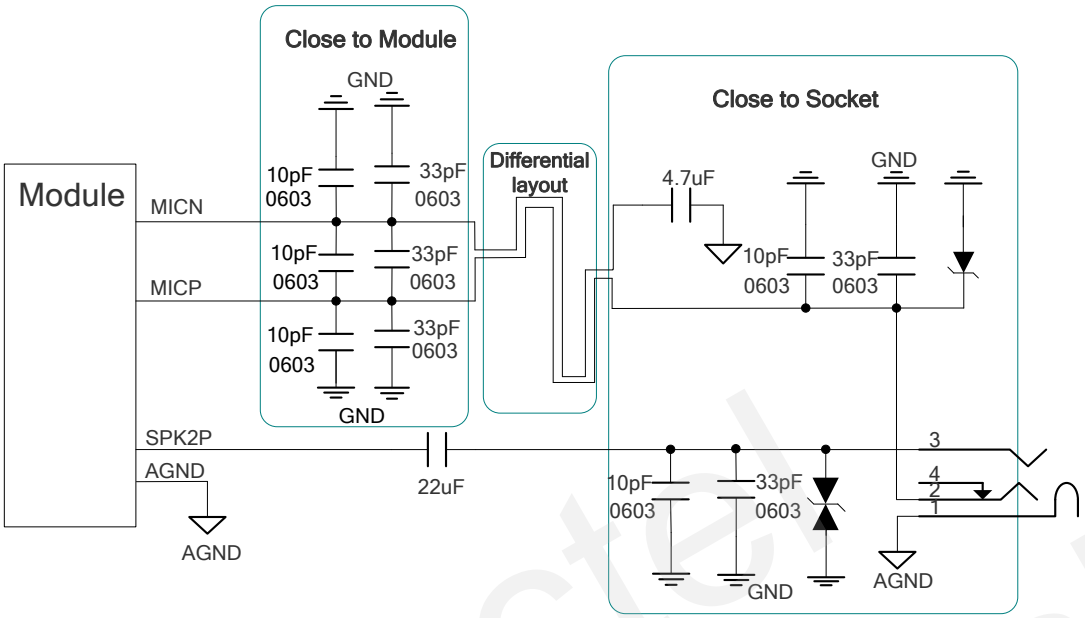

Figure 27: Reference Design for an Earphone

3.7.5. Audio Characteristics

Table 10: Typical Electret Microphone Characteristics

Parameter	Min.	Typ.	Max.	Unit
Working Voltage	1.2	1.5	2.0	V
Working Current	200		500	uA
External Microphone Load Resistance		2.2		k Ohm

Table 11: Typical Speaker Characteristics

Parameter			Min.	Typ.	Max.	Unit
AOUT1 Output	Single-ended	Load resistance		32		Ohm
		Ref level	0		2.4	Vpp
	Differential	Load resistance		32		Ohm

		Ref level	0		4.8	Vpp
AOUT2 Output	Single-ended	Load resistance		32		Load Resistance
		Reference level	0		2.4	Vpp

3.8. SIM Card Interface

The SIM interface supports the functionality of the GSM Phase 1 specification and also supports the functionality of the new GSM Phase 2+ specification for FAST 64kbps SIM card, which is intended for use with a SIM application Tool-kit.

The SIM interface is powered by an internal regulator in the module. Both 1.8V and 3.0V SIM Cards are supported.

Table 12: Pin Definition of the SIM Interface

Pin NO.	Name	Description	Alternate Function [1)]
14	SIM_VDD	Supply power for SIM card. Automatic detection of SIM card voltage: 3.0V±5% and 1.8V±5%. Maximum supply current is around 10mA.	
13	SIM_CLK	SIM card clock	
11	SIM_DATA	SIM card data I/O	
12	SIM_RST	SIM card reset	
19	SIM_PRESENCE	SIM card detection	DTR
10	SIM_GND	SIM card ground	

NOTE

[1)] If several interfaces share the same I/O pin, to avoid conflict between these alternate functions, only one peripheral should be enabled at a time.

The following figure is the reference design for SIM interface.

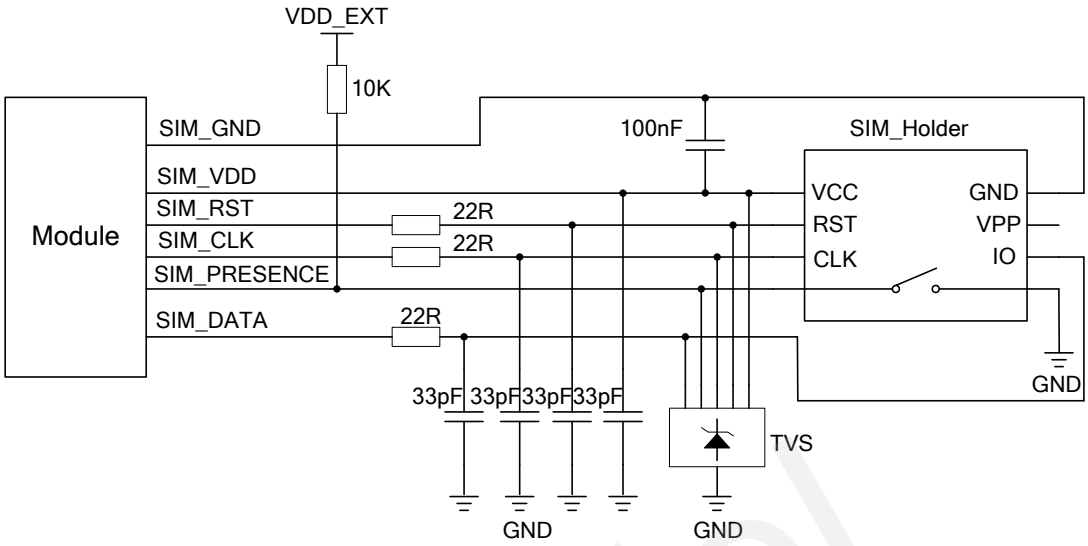

Figure 28: Reference Circuit for SIM Interface with 8-pin SIM Card Holder

If SIM card detection function is not used, keep SIM_PRESENCE pin open. The reference circuit for a 6-pin SIM card socket is illustrated as the following figure.

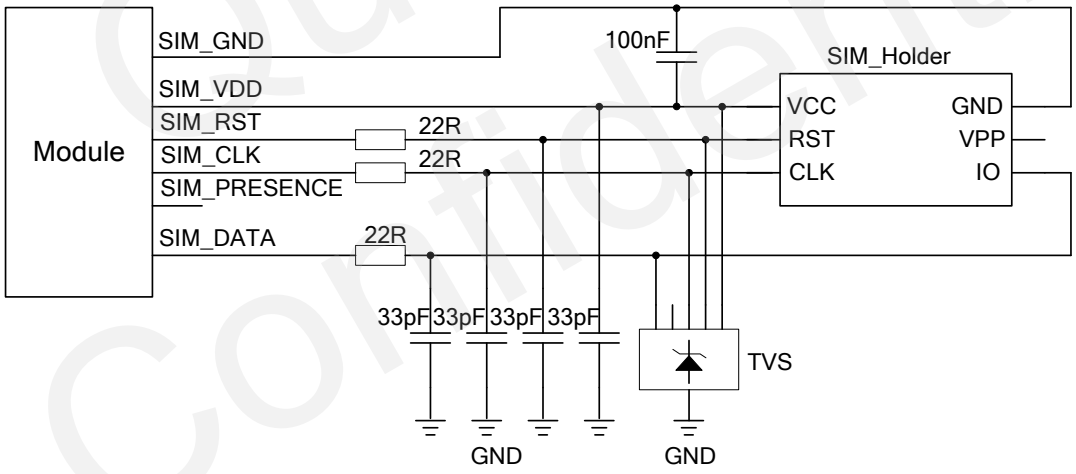

Figure 29: Reference Circuit for SIM Interface with the 6-pin SIM Card Holder

For more information of SIM card holder, you can visit http://www.amphenol.com and http://www.molex.com .

In order to enhance the reliability and availability of the SIM card in the customer's application, please follow the following rules in the SIM card circuit design.

- Keep layout of SIM card as close as possible to the module. Assure the possibility of the length of the

trace is less than 200mm.

- Keep SIM card signal away from RF and VBAT alignment.
- Assure the ground between module and SIM cassette short and wide. Keep the width of ground no less than 0.5mm to maintain the same electric potential. The decouple capacitor of SIM_VDD is less than 1uF and must be near to SIM cassette.
- To avoid cross talk between SIM_DATA and SIM_CLK. Keep them away with each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array. For more information of TVS diode, please visit http://www.onsemi.com/. The most important rule is to place the ESD protection device close to the SIM card socket and make sure the nets being protected will go through the ESD device first and then lead to module. The 22Ω resistors should be connected in series between the module and the SIM card so as to suppress the EMI spurious transmission and enhance the ESD protection. Please to be noted that the SIM peripheral circuit should be close to the SIM card socket.
- Place the RF bypass capacitors (33pF) close to the SIM card on all signals line for improving EMI.

3.9. SD Card Interface

The module provides an SD card interface that supports many types of memory, such as Memory Stick, SD/MCC card, and T-Flash or Micro SD card. The following are the main features of SD card interface.

- Only support 1bit serial mode
- Not support the SPI mode for SD memory card
- Not support multiple SD memory cards
- Not support hot plug
- The data rate up to 48MHz in serial mode
- Up to 32GB maximum memory card capacity

With the SD card interface features and reference circuit shown as below, you can easily design the SD card application circuit to enhance the memory capacity of the module. sers can store some high-capacity files to external memory card. Such as in the automotive application system, the module can record and store the audio file to the SD card, and also can play the audio files in SD card.

Table 13: Pin Definition of SD Card Interface

Pin Name	Pin No.	Description	Alternate Function [1)]
SD_CMD	32	Command signal of SD card output	PCM_IN
SD_CLK	33	Clock signal of SD card output	PCM_OUT

SD_DATA	31	Data output and input signal of SD card	PCM_SYNC

NOTE

1) If several interfaces share the same I/O pin, to avoid conflict between these alternate functions, only one peripheral should be enabled at a time.

A reference design for Micro SD card is shown below.

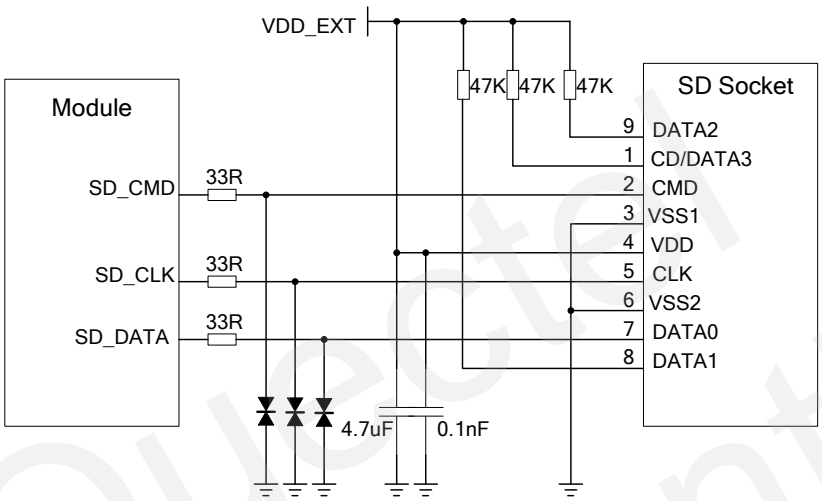

Figure 30: Reference Circuit for Micro SD Card

Table 14: Pin Name of the SD Card and T-Flash（Micro SD）Card

Pin No.	Pin Name of SD Card	Pin Name of T-Flash (Micro SD) Card
1	CD/DATA3	DATA2
2	CMD	CD/DATA3
3	VSS1	CMD
4	VDD	VDD
5	CLK	CLK
6	VSS2	VSS
7	DATA0	DATA0
8	DATA1	DATA1

9	DATA2

In SD card interface designing, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- Keep all the SD card signals far away from VBAT power and RF trace.
- Route all SD card signals as short as possible. Ensure the length of every trace does not exceed 10cm.
- The SD_CLK, SD_DATA and SD_CMD trace should be routed together. Keep trace difference of SD_DATA, SD_CMD and SD_CLK to be less than 10mm.
- In order to offer good ESD protection, it is recommended to add TVS on signals with capacitance less than 15pF.
- Reserve external pull-up resistors for other data lines except the DATA0 signal.
- The SD_CLK and SD_DATA line must be shielded by ground in order to improve EMI suppression capability.

3.10. PCM Interface

M66-OpenCPU supports PCM interface. It is used for digital audio transmission between the module and the device. This interface is composed of PCM_CLK, PCM_SYNC, PCM_IN and PCM_OUT signal lines.

Pulse-code modulation (PCM) is a converter that changes the consecutive analog audio signal to discrete digital signal. The whole procedure of pulse-code modulation contains sampling, quantizing and encoding.

Table 15: Pin Definition of PCM Interface

Pin NO.	Pin Name	Description
30	PCM_CLK	PCM clock output
31	PCM_SYNC	PCM frame synchronization output
32	PCM_IN	PCM data input
33	PCM_OUT	PCM data output

NOTE

If the PCM function is not used, these pins can be used as GPIOs. For detailed information about GPIO, please refer to Section ***3.15 GPIO***.

3.10.1. Configuration

M66-DS-OpenCPU module supports 16-bit line code PCM format. The sample rate is 8 KHz; the clock source is 256 KHz; and the module can only act as master mode. The PCM interface supports both long and short synchronization. Furthermore, it only supports MSB first. For detailed information, please refer to the table below.

Table 16: Configuration

PCM	
Line Interface Format	Linear
Data Length	Linear: 16 bits
Sample Rate	8KHz
PCM Clock/Synchronization Source	PCM master mode: clock and synchronization is generated by module
PCM Synchronization Rate	8KHz
PCM Clock Rate	PCM master mode: 256 KHz (line)
PCM Synchronization Format	Long/short synchronization
PCM Data Ordering	MSB first
Zero Padding	NO
Sign Extension	NO

3.10.2. Timing

The sample rate of the PCM interface is 8 KHz and the clock source is 256 KHz, so every frame contains 32 bits data. M66-DS-OpenCPU supports 16 bits line code PCM format. The left 16 bits are valid, and the data of the left 16 bits and the right 16 bits are the same. The following diagram shows the timing of different combinations. The synchronization length in long synchronization format can be programmed by firmware from one bit to eight bits.

You can configure the PCM input and output volume by executing **AT+QPCMVOL** command. For more details, please refer to ***Chapter 3.10.4***

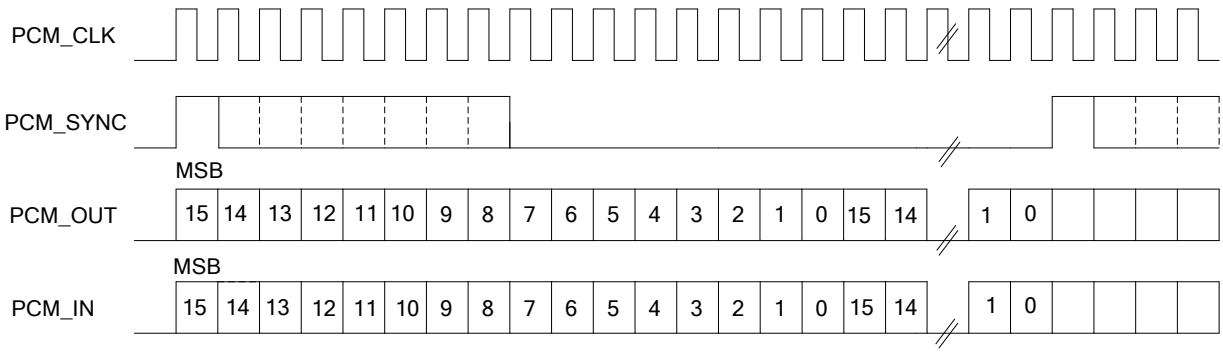

Figure 31: Long Synchronization Diagram

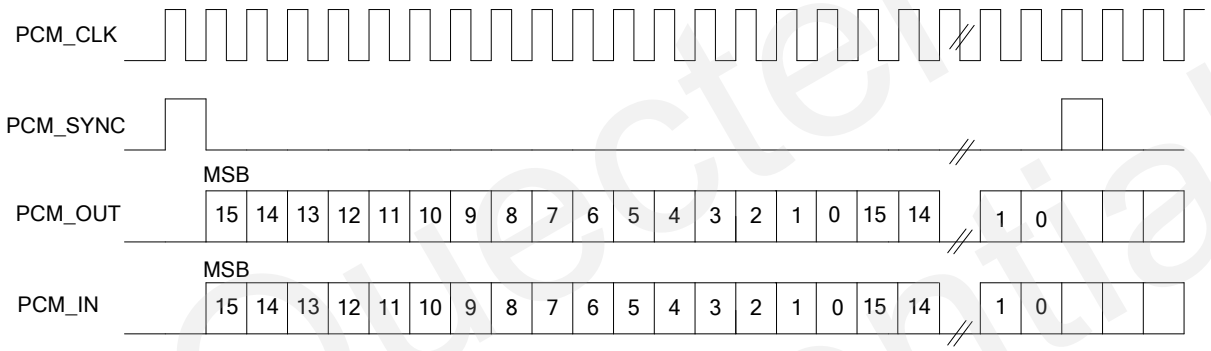

Figure 32: Short Synchronization Diagram

3.10.3. Reference Design

As M66-OpenCPU can only act as a master, the module provides synchronization and clock source. The reference design is shown as below.

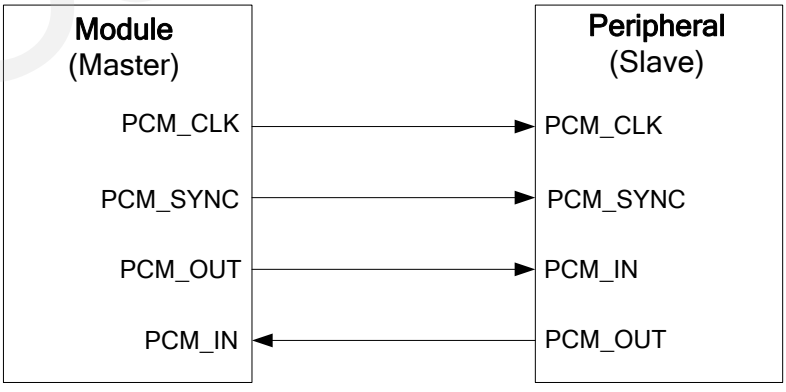

Figure 33: Reference Design for PCM

3.10.4. AT Command

There are two AT commands to configure PCM, listed as below.

AT+QPCMON can configure operating mode of PCM.

AT+QPCMON=mode, Sync_Type, Sync_Length, SignExtension, MSBFirst.

Table 17: QPCMON Command Description

Parameter	Scope	Description
Mode	0,2	0: Close PCM 2: Open PCM when audio talk is set up
Sync_Type	0~1	0: Short synchronization 1: Long synchronization
Sync_Length	1~8	Programmed from one bit to eight bits
SignExtension	0~1	Not supported
MSBFirst	0~1	0: MSB first 1: Not supported

AT+QPCMVOL can configure the volume of input and output.

AT+QPCMVOL=vol_pcm_in, vol_pcm_out

Table 18: QPCMVOL Command Description

Parameter	Scope	Description
vol_pcm_in	0~32767	Set the input volume
vol_pcm_out	0~32767	Set the output volume The voice may be distorted when this value exceeds 16384.

3.11. SPI and I2C Interface

M66-OpenCPU module supports SPI and I2C interface.

3.11.1. SPI Interface

SPI interface is multiplexed by PCM interface. SPI interface of M66-OpenCPU is master only. It provides a duplex, synchronous and serial communication link with the peripheral devices. Its operation voltage is 2.8V, with clock rates up to 10MHZ. Main features for the SPI interface are as below.

- Support master mode operation
- Adjustable clock speed
- Serial clock with programmable polarity and phase

The logic levels of SPI interfaces are described in the following table.

Table 19: Logic Levels of the SPI Interface

Parameter	Min.	Max.	Unit
V_{IL}	0	0.25×VDD_EXT	V
V_{IH}	0.75×VDD_EXT	VDD_EXT +0.2	V
V_{OL}	0	0.15×VDD_EXT	V
V_{OH}	0.85×VDD_EXT	VDD_EXT	V

Table 20: Pin Definition of the SPI Interface

Pin NO.	Name	Description	Alternate Function [1)]
33	SPI_MOSI	Master output, Slave input of SPI Interface	PCM_OUT
32	SPI_CLK	Clock signal of SPI interface	PCM_IN
31	SPI_MISO	Master input, Slave output of SPI Interface	PCM_SYNC
30	SPI_CS	Chip select of SPI Interface	PCM_CLK

NOTE

[1)] If several interfaces share the same I/O pin, to avoid conflict between these alternate functions, only one peripheral should be enabled at a time.

The M66-OpenCPU SPI must be configured as the master. The API functions of the file system can be used to read/write SPI. For detailed information about software design, please refer to the ***document***

[12].

3.11.2. I2C Interface

I2C is a two-wire serial interface which is multiplexed by RI and DCD pins. The two signals are SCL and SDA. Main features for the I2C interface are as below.

- Support master mode operation
- Adjustable clock speed for LS/FS mode operation
- Supports 7-bit addressing
- Supports high speed mode

Table 21: Logic Levels of the I2C Interface

Parameter	Min.	Max.	Unit
V_{IL}	0	0.25×VDD_EXT	V
V_{IH}	0.75×VDD_EXT	VDD_EXT +0.2	V
V_{OL}	0	0.15×VDD_EXT	V
V_{OH}	0.85×VDD_EXT	VDD_EXT	V

Table 22: Pin Definition of the I2C Interface

Pin NO.	Name	Description	Comment	Alternate Function [1)]
20	I2C_SCL	I2C serial clock	Require external pull-up resistor	RI
21	I2C_SDA	I2C serial data		DCD

NOTE

[1)] If several interfaces share the same I/O pin, to avoid conflict between these alternate functions, only one peripheral should be enabled at a time.

The API functions of the file system can be used to read/write I2C. For detailed information about software design, please refer to the ***document [12]***.

3.12. ADC

The module provides an ADC input channels to measure the value of voltage. The API function **Ql_ADC_Sampling()** can be used to read the voltage value from ADC input channel. For detailed information about software design, please refer to the ***document [12]***.

Table 23: Pin Definition of the ADC

Pin NO.	Pin Name	Description
8	AVDD	Reference voltage of ADC circuit
9	ADC0	Analog to digital converter.

Table 24: Characteristics of the ADC

Item	Min.	Typ.	Max.	Unit
Voltage Range	0		2.8	V
ADC Resolution		10		bits
ADC Accuracy		2.7		mV

NOTE

If the voltage value from ADC input channel is greater than 2.8V, it will be read as 2.8V only by **Ql_ADC_Sampling()**. So you need to keep the voltage value of ADC less than 2.8V by voltage divider.

3.13. External Interrupt

M66-OpenCPU module possesses one external interrupt which can support level trigger. External interrupt is multiplexed function, and when their default functions are not used, they can be configured as external interrupt.

Table 25: Pin List for External Interrupt

Pin NO.	Pin Name	Trigger Type
19	DTR	Level

If an external interrupt occurs, the previously registered interrupt callback function will be invoked. For detailed information about software design, please refer to the ***document [12]***.

NOTE

If external interrupt is not used, related pins can be multiplexed as GPIO. For detailed information about GPIO, please refer to Section ***3.15 GPIO***.

3.14. PWM

M66-OpenCPU module provides a PWM signal output channel which is called NETLIGHT. NETLIGHT indicates network status by default and it can also be configured by related API function. The working status for NETLIGHT is shown in the following table.

Table 26: Working Status for NETLIGHT

State	Module Function
Off	The module is not running.
64ms On/800ms Off	The module is not synchronized with network.
64ms On/2000ms Off	The module is synchronized with network.
64ms On/600ms Off	The GPRS data transmission.

Reference design for NETLIGHT is shown as below.

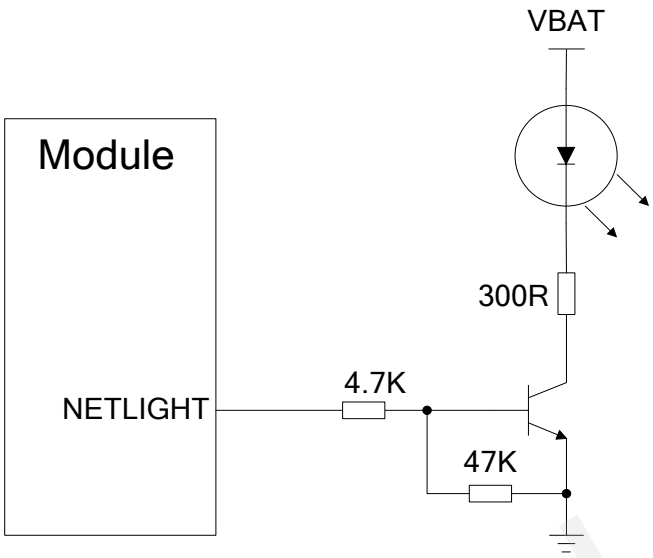

Figure 34: Reference Design for NETLIGHT

Furthermore, PWM signal parameters can be configured by calling the API function **Ql_PWM_Output()**. For detailed information about software design, please refer to the ***document [12]***.

3.15. GPIO

M66-OpenCPU module provides 12 GPIOs in all. In order to reduce the pin number, GPIO is multiplexed with other functions. When pin's default function is not used, it can be configured as GPIO. API functions, such as **Ql_GPIO_Init**, **Ql_GPIO_SetLevel**, **Ql_GPIO_SetDirection**, **Ql_GPIO_SetPullSelection**, can be used for GPIO operation. For detailed information about software design, please refer to the ***document [12]***.

Table 27: Pin List for GPIO

Pin No.	Name	Mode	Reset		Output Driving
			I/O	PU/PD	
16	NETLIGHT	Mode 2	I	PD	4mA
19	DTR	Mode 2	I	PD	4mA
20	RI	Mode 2	I	PD	4mA
21	DCD	Mode 2	I	PD	4mA

22	CTS	Mode 2	I	PU	4mA
23	RTS	Mode 2	I	PU	4mA
28	RXD_AUX	Mode 2	I	PD	4mA
29	TXD_AUX	Mode 2	I	PD	4mA
30	PCM_CLK	Mode 2	HO	-	4mA
31	PCM_SYNC	Mode 2	I	PD	4mA
32	PCM_IN	Mode 2	I	PU	4mA
33	PCM_OUT	Mode 2	I	PD	4mA

If you configure GPIO as input or output port, please pay attention to level match when the module is connected with other peripherals. The reference design for 3.3V level match is shown as below.

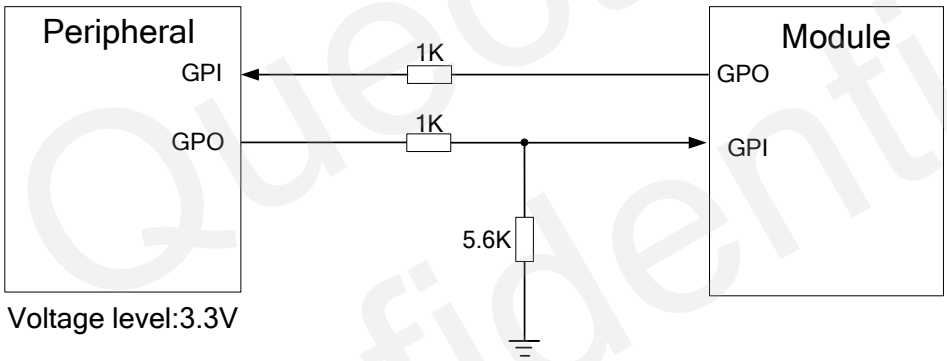

Figure 35: GPIO Level Match Design for 3.3V System

NOTE

If the digital I/O between customer and module does not match, it will cause some unexpected result. So it is highly recommended to add the level match circuit when the module is connected with other peripherals. For more details about digital IO application, please refer to ***document [14]***.

3.16. RF Transmitting Signal Indication

The M66-OpenCPU provides a RFTXMON pins which will rise when the transmitter is active and fall after the transmitter activity is completed.

Table 28: Pin Definition of the RFTXMON

Pin Name	Pin No.	Description
RFTXMON	25	Transmission signal indication

There are two different modes for this function:

1. Active during the TX activity

RFTXMON pin is used to indicate the TX burst, when it outputs a high level, 220us later there will be a TX burst.

You can execute **AT+QCFG="RFTXburst", 1** to enable the function. The timing of the RFTXMON signal is shown below.

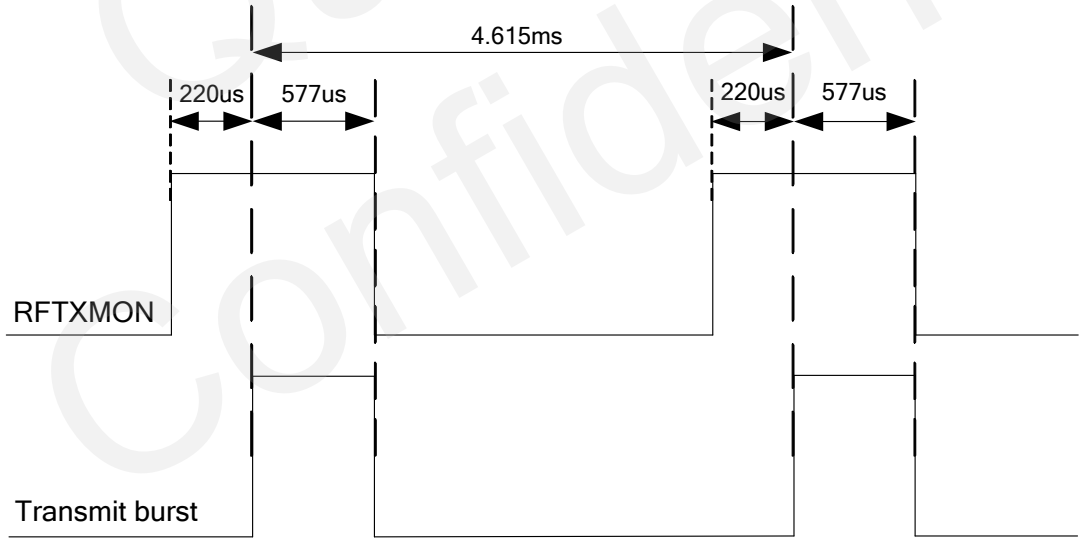

Figure 36: RFTXMON Signal during Burst Transmission

2. Active during the Call

RFTXMON will be HIGH during a call and the pin will become LOW after hanged up.

You can execute **AT+QCFG="RFTXburst", 2** to enable the function. The timing of the RFTXMON signal is shown below.

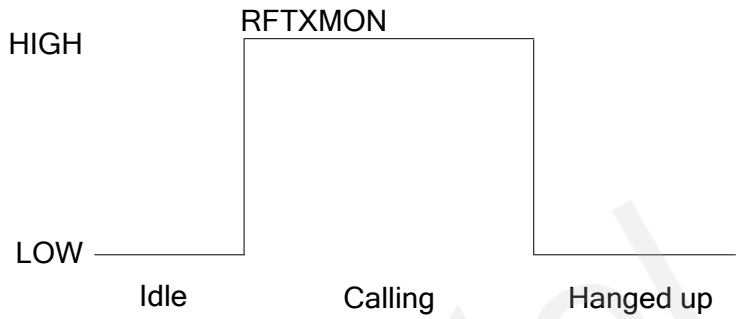

Figure 37: RFTXMON Signal during Calling

4 Antenna Interface

M66-OpenCPU has two antenna interfaces, GSM antenna and BT antenna. The pin 26 is the Bluetooth antenna pad. The pin 35 is the GSM antenna pad. The RF interface of the two antenna pad has an impedance of 50Ω.

4.1. GSM Antenna Interface

There is a GSM antenna pad named RF_ANT for M66-OpenCPU.

Table 29: Pin Definition of the RF_ANT

Name	Pin	Description
GND	34	Ground
RF_ANT	35	GSM antenna pad
GND	36	Ground
GND	37	Ground

4.1.1. Reference Design

The external antenna must be matched properly to achieve best performance, so the matching circuit is necessary, the reference design for RF is shown as below.

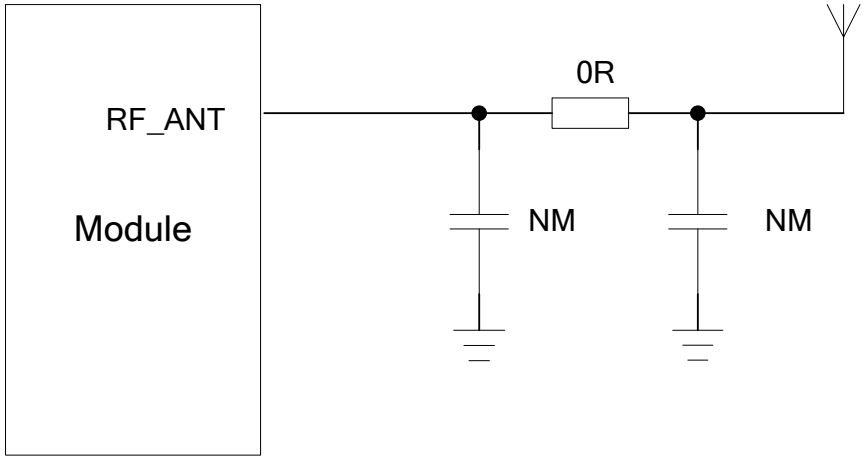

Figure 38: Reference Design for GSM Antenna

M66-OpenCPU provides an RF antenna pad for antenna connection. The RF trace in host PCB connected to the module RF antenna pad should be coplanar waveguide line or microstrip line, whose characteristic impedance should be close to 50Ω. M66-OpenCPU comes with grounding pads which are next to the antenna pad in order to give a better grounding. Besides, a π type match circuit is suggested to be used to adjust the RF performance.

To minimize the loss on the RF trace and RF cable, please pay attention to the design. The following table shows the requirement on GSM antenna.

Table 30: Antenna Cable Requirements

Type	Requirements
GSM850/EGSM900	Cable insertion loss <1dB
DCS1800/PCS1900	Cable insertion loss <1.5dB

Table 31: Antenna Requirements

Type	Requirements
Frequency Range	Depending by frequency band (s) provided by the network operator
VSWR	≤ 2
Gain (dBi)	1
Max Input Power (W)	50

Input Impedance (Ω)	50
Polarization Type	Vertical

4.1.2. RF Output Power

Table 32: The Module Conducted RF Output Power

Frequency	Max.	Min.
GSM850	33dBm±2dB	5dBm±5dB
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB

NOTE

In GPRS 4 slots TX mode, the max output power is reduced by 2.5dB. This design conforms to the GSM specification as described in section ***13.16*** of ***3GPP TS 51.010-1***.

4.1.3. RF Receiving Sensitivity

Table 33: The Module Conducted RF Receiving Sensitivity

Frequency	Receive Sensitivity
GSM850	< -109dBm
EGSM900	< -109dBm
DCS1800	< -109dBm
PCS1900	< -109dBm

4.1.4. Operating Frequencies

Table 34: The Module Operating Frequencies

Frequency	Receive	Transmit	ARFCH
GSM850	869~894MHz	824~849MHz	128~251
EGSM900	925~960MHz	880~915MHz	0~124, 975~1023
DCS1800	1805~1880MHz	1710~1785MHz	512~885
PCS1900	1930~1990MHz	1850~1910MHz	512~810

4.1.5. RF Cable Soldering

Soldering the RF cable to RF pad of module correctly will reduce the loss on the path of RF, please refer to the following example of RF soldering.

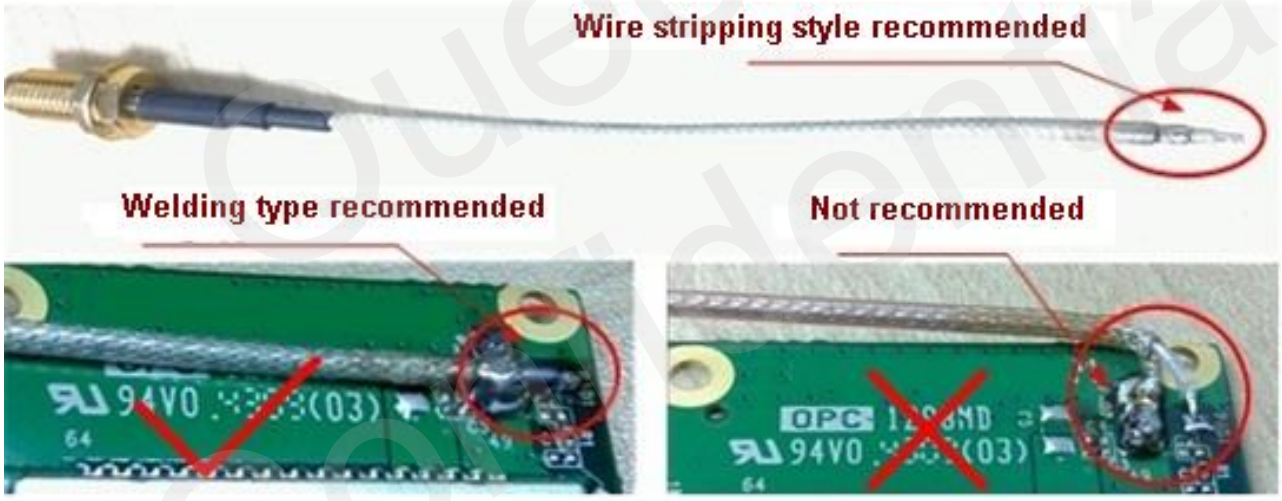

Figure 39: RF Soldering Sample

4.2. Bluetooth Antenna Interface

M66-OpenCPU supports Bluetooth interface. Bluetooth is a wireless technology that allows devices to communicate, or transmit data or voice, wirelessly over a short distance. It is described as a short-range communication technology intended to replace the cables connecting portable and/or fixed devices while maintaining high level of security. Bluetooth is standardized as IEEE802.15 and operates in the 2.4 GHz range using RF technology. Its data rates up to 3Mbps.

M66-OpenCPU is fully compliant with Bluetooth specification 3.0. It supports profile including SPP and OPP.

The module provides a Bluetooth antenna pad named BT_ANT.

Table 35: Pin Definition of the BT_ANT

Name	Pin	Description
BT_ANT	26	BT antenna pad
GND	27	Ground

The external antenna must be matched properly to achieve best performance, so the matching circuit is necessary, the connection is recommended as the following figure.

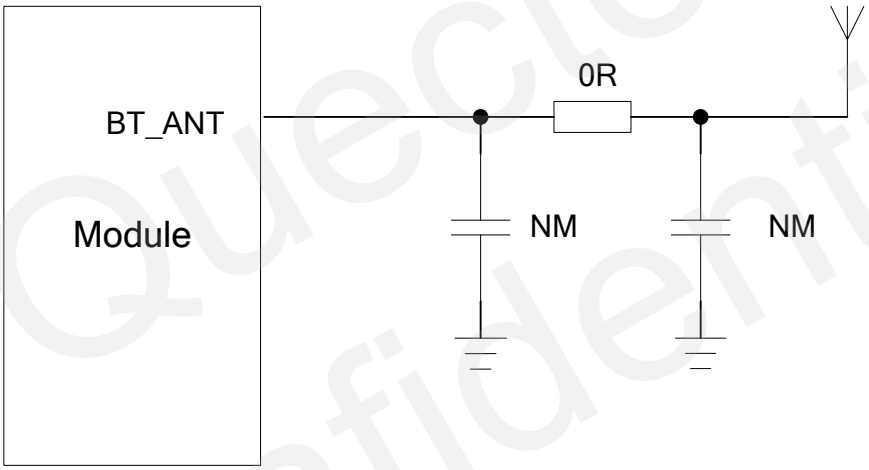

Figure 40: Reference Design for Bluetooth Antenna

There are some suggestions for placing components and RF trace lying for Bluetooth RF traces:

- Antenna matching circuit should be closed to the antenna;
- Keep the RF traces as 50Ω;
- The RF traces should be kept far away from the high frequency signals and strong disturbing source.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of module are listed in the following table.

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	+4.73	V
Peak Current of Power Supply	0	2	A
RMS Current of Power Supply (during one TDMA- frame)	0	0.7	A
Voltage at Digital Pins	-0.3	3.08	V
Voltage at Analog Pins	-0.3	3.08	V
Voltage at Digital/analog Pins in Power Down Mode	-0.25	0.25	V

5.2. Operating Temperature

The operating temperature is listed in the following table.

Table 37: Operating Temperature

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature	-35	+25	+75	ºC

Extended Temperature	-40	+85	ºC

NOTES

1. [1] Within operation temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction; there are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP compliant again.

5.3. Power Supply Ratings

Table 38: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	Supply voltage	Voltage must stay within the min/max values, including voltage drop, ripple, and spikes.	3.3	4.0	4.6	V
	Voltage drop during transmitting burst	Maximum power control level on GSM850 and EGSM900.			400	mV
I_{VBAT}	Average supply current	Power down mode		150		uA
		SLEEP mode @DRX=5		1.3		mA
		Minimum functionality mode AT+CFUN=0				
		IDLE mode		13		mA
		SLEEP mode		0.98		mA
		AT+CFUN=4				
		IDLE mode		13		mA
		SLEEP mode		1.0		mA
		TALK mode				
		GSM850/EGSM 900[1]		223/219		mA
		DCS1800/PCS1900[2]		153/151		mA
		DATA mode, GPRS (3Rx, 2Tx)				
		GSM850/EGSM 900[1]		363/393		mA
		DCS1800/PCS1900[2]		268/257		mA
		DATA mode, GPRS (2 Rx,3Tx)				

		GSM850/EGSM 900[1)] DCS1800/PCS1900[2)]	506/546 366/349		mA mA
		DATA mode, GPRS (4 Rx,1Tx) GSM850/EGSM 900[1)] DCS1800/PCS1900[2)]	 217/234 172/170		 mA mA
		DATA mode, GPRS (1Rx,4Tx) GSM850/EGSM 900[1)] DCS1800/PCS1900[2)]	 458/485[3)] 462/439		 mA mA
	Peak supply current (during transmission slot)	Maximum power control level on GSM850 and EGSM900.	1.6	2	A

NOTES

1. [1)] Power control level PCL 5.
2. [2)] Power control level PCL 0.
3. [3)] Under the GSM850 and EGSM900 spectrum, the power of 1Rx and 4Tx has been reduced.

5.4. Current Consumption

The values of current consumption are shown as below.

Table 39: The Module Current Consumption

Condition	Current Consumption
Voice Call	
GSM850	@power level #5 <300mA, Typical 223mA @power level #12, Typical 83mA @power level #19, Typical 62mA
EGSM900	@power level #5 <300mA, Typical 219mA @power level #12, Typical 83mA @power level #19, Typical 63mA
DCS1800	@power level #0 <250mA, Typical 153mA @power level #7, Typical 73mA @power level #15, Typical 60mA
PCS1900	@power level #0 <250mA, Typical 151mA @power level #7, Typical 76mA

	@power level #15, Typical 61mA
GPRS Data	
DATA Mode, GPRS (3 Rx, 2Tx) CLASS 12	
GSM850	@power level #5 <550mA, Typical 363mA @power level #12, Typical 131mA @power level #19, Typical 91mA
EGSM900	@power level #5 <550mA, Typical 393mA @power level #12, Typical 132mA @power level #19, Typical 92mA
DCS1800	@power level #0 <450mA, Typical 268mA @power level #7, Typical 112mA @power level #15, Typical 88mA
PCS1900	@power level #0 <450mA, Typical 257mA @power level #7, Typical 119mA @power level #15, Typical 89mA
DATA Mode, GPRS (2 Rx, 3Tx) CLASS 12	
GSM850	@power level #5 <640mA, Typical 506mA @power level #12, Typical 159mA @power level #19, Typical 99mA
EGSM900	@power level #5 <600mA, Typical 546mA @power level #12, Typical 160mA @power level #19, Typical 101mA
DCS1800	@power level #0 <490mA, Typical 366mA @power level #7, Typical 131mA @power level #15, Typical 93mA
PCS1900	@power level #0 <480mA, Typical 348mA @power level #7, Typical 138mA @power level #15, Typical 94mA
DATA Mode, GPRS (4 Rx,1Tx) CLASS 12	
GSM850	@power level #5 <350mA, Typical 216mA @power level #12, Typical 103mA @power level #19, Typical 83mA
EGSM900	@power level #5 <350mA, Typical 233mA @power level #12, Typical 104mA @power level #19, Typical 84mA
DCS1800	@power level #0 <300mA, Typical 171mA @power level #7, Typical 96mA @power level #15, Typical 82mA
PCS1900	@power level #0 <300mA, Typical 169mA

	@power level #7, Typical 98mA @power level #15, Typical 83mA
DATA Mode, GPRS (1 Rx, 4Tx) CLASS 12	
GSM850	@power level #5 <660mA, Typical 457mA @power level #12, Typical 182mA @power level #19, Typical 106mA
EGSM900	@power level #5 <660mA, Typical 484mA @power level #12, Typical 187mA @power level #19, Typical 109mA
DCS1800	@power level #0 <530mA, Typical 461mA @power level #7, Typical 149mA @power level #15, Typical 97mA
PCS1900	@power level #0 <530mA, Typical 439mA @power level #7, Typical 159mA @power level #15, Typical 99mA

NOTE

GPRS Class 12 is the default setting. The module can be configured from GPRS Class 1 to Class 12. Setting to lower GPRS class would make it easier to design the power supply for the module.

5.5. Electro-static Discharge

Although the GSM engine is generally protected against Electro-static Discharge (ESD), ESD protection precautions should still be emphasized. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any applications using the module.

The measured ESD values of module are shown as the following table.

Table 40: The ESD Endurance (Temperature: 25ºC, Humidity: 45%)

Tested Point	Contact Discharge	Air Discharge
VBAT, GND	±5KV	±10KV
RF_ANT	±5KV	±10KV
TXD, RXD	±2KV	±4KV
Others	±0.5KV	±1KV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module.

6.1. Mechanical Dimensions of Module

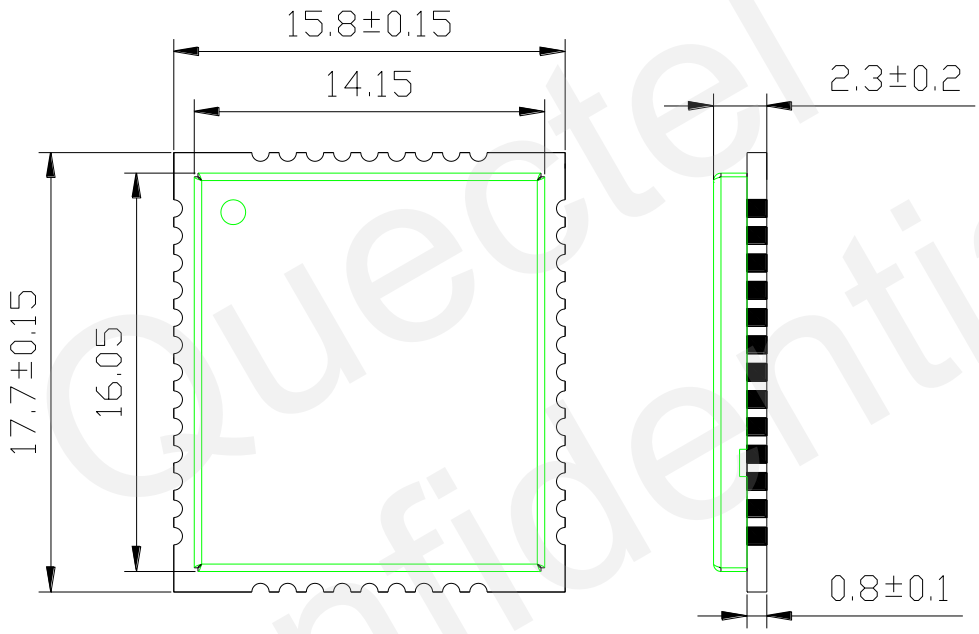

Figure 41: M66-OpenCPU Module Top and Side Dimensions (Unit: mm)

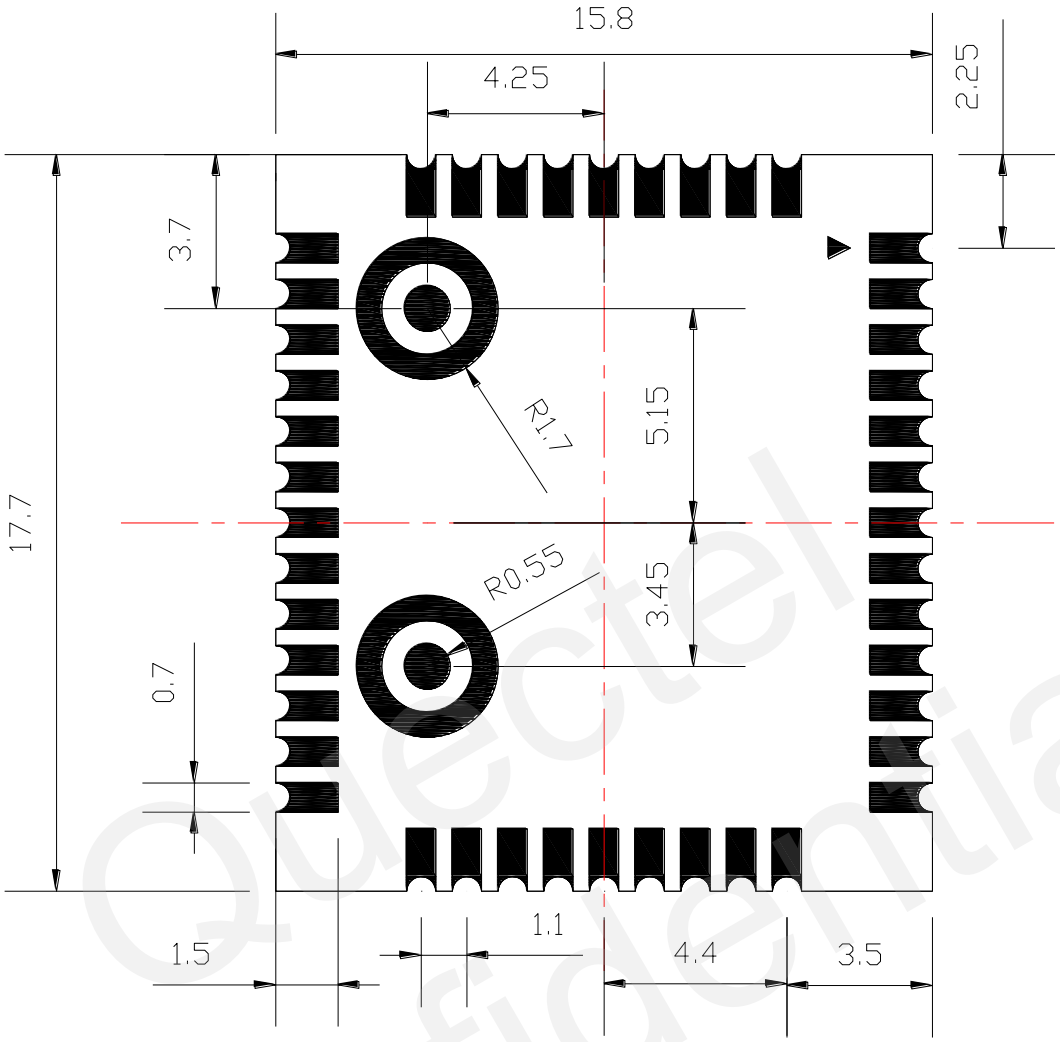

Figure 42: M66-OpenCPU Module Bottom Dimensions (Unit: mm)

6.2. Recommended Footprint

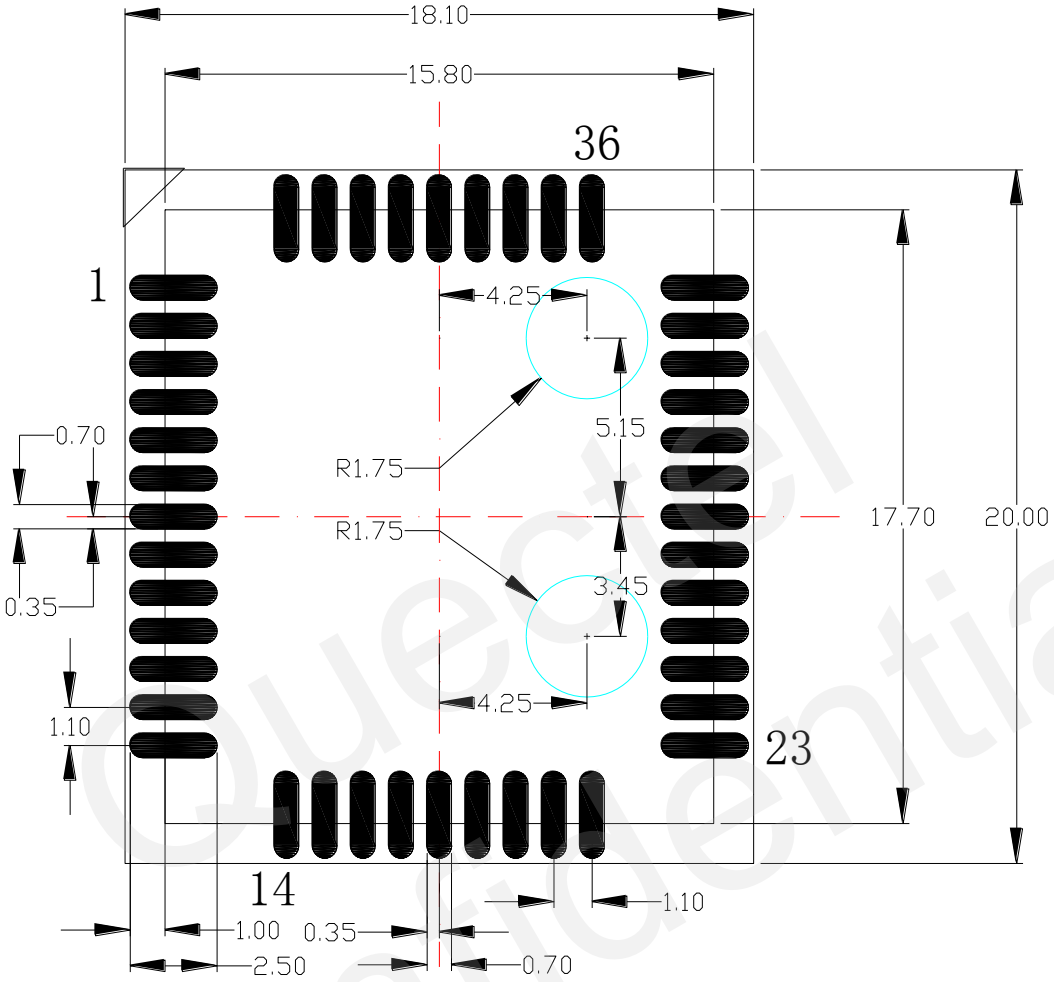

Figure 43: Recommended Footprint (Unit: mm)

NOTES

1. The module should be kept about 3mm away from other components in the host PCB.
2. The circular test points with a radius of 1.75mm in the above recommended footprint should be treated as keepout areas. (“keepout” means do not pour copper on the mother board).

6.3. Top View of the Module

Figure 44: Top View of the Module

6.4. Bottom View of the Module

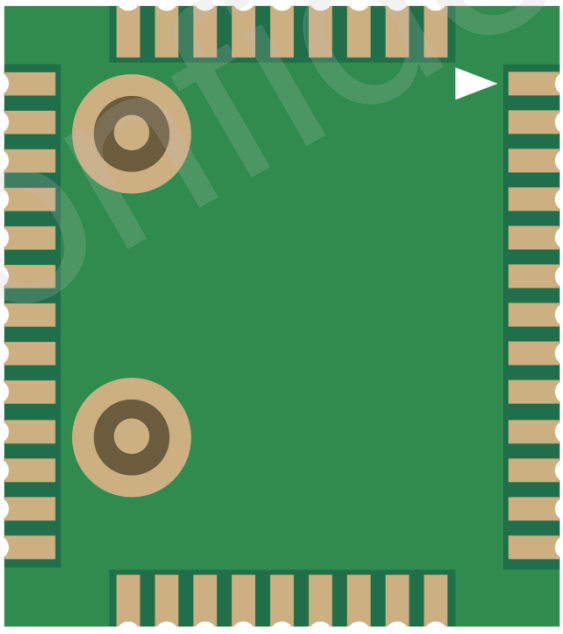

Figure 45: Bottom View of the Module

7 Storage and Manufacturing

7.1. Storage

M66-OpenCPU module is stored in a vacuum-sealed bag. The storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC and <90%RH.

2. After the vacuum-sealed bag is opened, devices that need to be mounted directly must be:

- Mounted within 72 hours at the factory environment of ≤30ºC and <60% RH.
- Stored at <10% RH.

3. Devices require baking before mounting, if any circumstance below occurs.

- When the ambient temperature is 23ºC±5ºC and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
- Device mounting cannot be finished within 72 hours when the ambient temperature is <30ºC and the humidity is <60%.
- Stored at >10% RH.

4. If baking is required, devices should be baked for 48 hours at 125ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (125ºC) baking. If shorter baking time is desired, please refer to IPC/JEDECJ-STD-033 for baking procedure.

7.2. Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the

thickness of stencil at the hole of the module pads should be 0.2 mm M66-OpenCPU. For more details, please refer to ***document [13]***.

It is suggested that peak reflow temperature is from 235ºC to 245ºC (for SnAg3.0Cu0.5 alloy). The absolute max reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below:

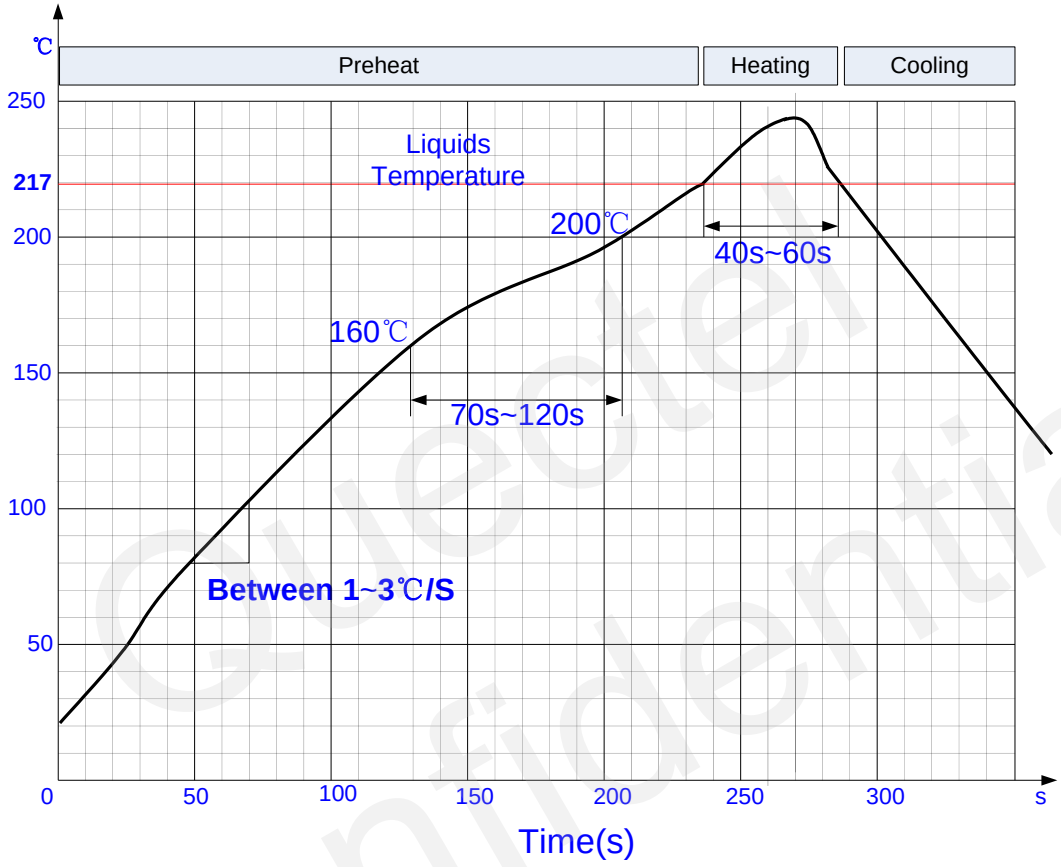

Figure 46: Reflow Soldering Thermal Profile

7.3. Packaging

The modules are stored in a vacuum-sealed bag which is ESD protected. It should not be opened until the devices are ready to be soldered onto the application.

7.3.1. Tape and Reel Packaging

The reel is 330mm in diameter and each reel contains 250 modules.

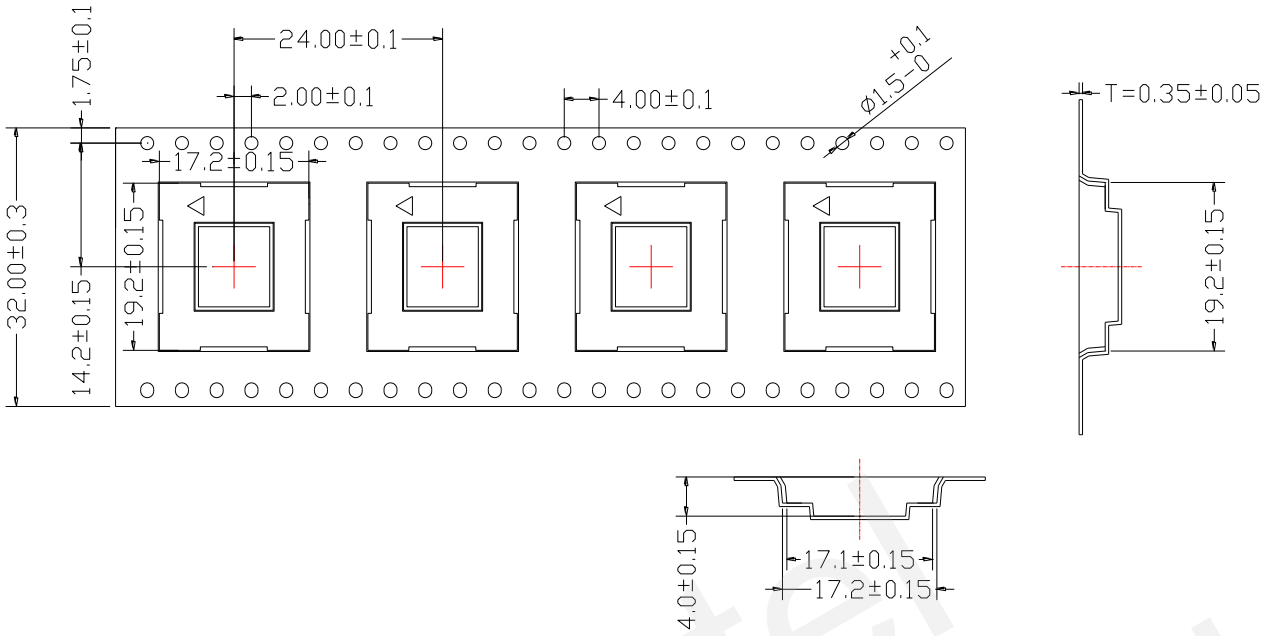

Figure 47: Tape and Reel Specification

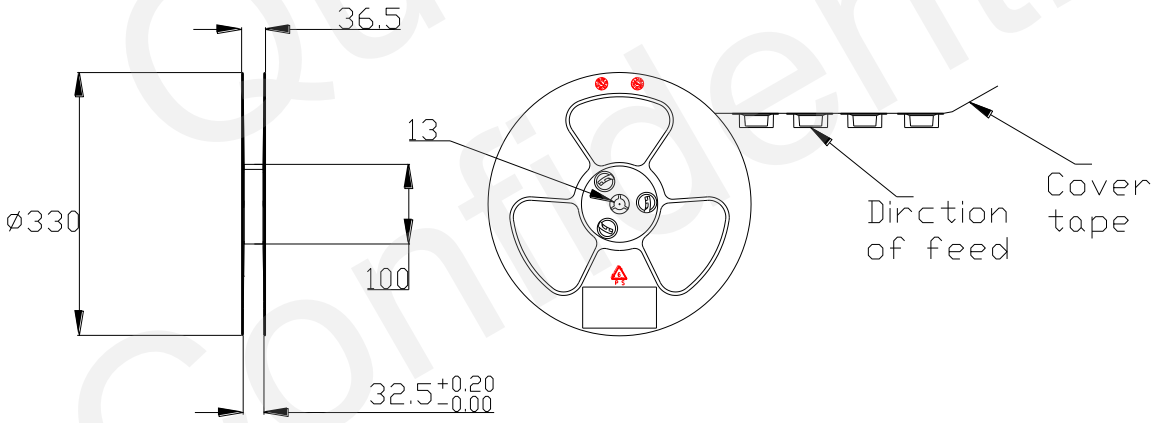

Figure 48: Dimensions of Reel

8 Appendix A References

Table 41: Related Documents

SN	Document Name	Remark
[1]	Quectel_M66_AT_Commands_Manual	AT commands manual
[2]	ITU-T Draft new recommendation V.25ter	Serial asynchronous automatic dialing and control
[3]	GSM 07.07	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[4]	GSM 07.10	Support GSM 07.10 multiplexing protocol
[5]	GSM 07.05	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[6]	GSM 11.14	Digital cellular telecommunications (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity module – Mobile Equipment (SIM – ME) interface
[7]	GSM 11.11	Digital cellular telecommunications (Phase 2+); Specification of the Subscriber Identity module – Mobile Equipment (SIM – ME) interface
[8]	GSM 03.38	Digital cellular telecommunications (Phase 2+); Alphabets and language-specific information
[9]	GSM 11.10	Digital cellular telecommunications (Phase 2); Mobile Station (MS) conformance specification; Part 1: Conformance specification
[10]	GSM_UART_AN	UART port application notes
[11]	GSM_EVB_UGD	GSM EVB user guide
[12]	OpenCPU_User_Guide	Software design reference for OpenCPU
[13]	Module_Secondary_SMT_User_Guide	Module secondary SMT user guide

[14]	Quectel_GSM_Module_Digital_IO_Application_Note	GSM Module Digital IO application note

Table 42: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
ARP	Antenna Reference Point
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
BOM	Bill Of Material
BTS	Base Transceiver Station
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital-to-Analog Converter
DRX	Discontinuous Reception
DSP	Digital Signal Processor
DCE	Data Communications Equipment (typically module)
DTE	Data Terminal Equipment (typically computer, external controller)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge

ETS	European Telecommunication Standard
FCC	Federal Communications Commission (U.S.)
FDMA	Frequency Division Multiple Access
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GPRS	General Packet Radio Service
GPI	General Purpose Input
GPO	General Purpose Output
GSM	Global System for Mobile Communications
HO	High output
HR	Half Rate
I/O	Input/Output
L/H	Low/High
PU/PD	Pull up/Pull down
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
Inorm	Normal Current
kbps	Kilo Bits Per Second
LED	Light Emitting Diode
Li-Ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol

PBCCH	Packet Switched Broadcast Control Channel
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RTC	Real Time Clock
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
UART	Universal Asynchronous Receiver&Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio
$V_O$max	Maximum Output Voltage Value
$V_O$norm	Normal Output Voltage Value
$V_O$min	Minimum Output Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value

$V_I$norm	Absolute Normal Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
Phonebook Abbreviations	
LD	SIM Last Dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT Calls (missed calls)
ON	SIM (or ME) Own Numbers (MSISDNs) list
RC	Mobile Equipment list of Received Calls
SM	SIM phonebook

9 Appendix B GPRS Coding Schemes

Four coding schemes are used in GPRS protocol. The differences between them are shown in the following table.

Table 43: Description of Different Coding Schemes

Scheme	Code Rate	USF	Pre-coded USF	Radio Block excl.USF and BCS	BCS	Tail	Coded Bits	Punctured Bits	Data Rate Kb/s
CS-1	1/2	3	3	181	40	4	456	0	9.05
CS-2	2/3	3	6	268	16	4	588	132	13.4
CS-3	3/4	3	6	312	16	4	676	220	15.6
CS-4	1	3	12	428	16	-	456	-	21.4

Radio block structure of CS-1, CS-2 and CS-3 is shown as the figure below.

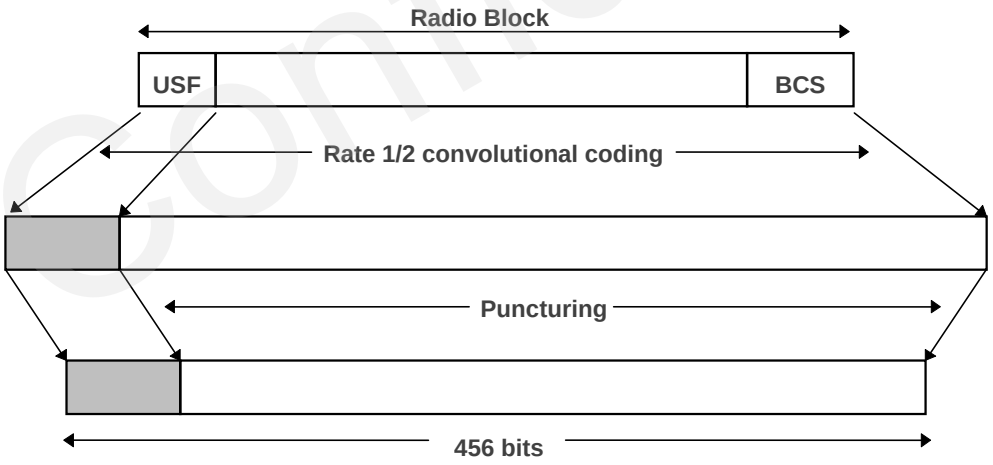

Figure 49: Radio Block Structure of CS-1, CS-2 and CS-3

Radio block structure of CS-4 is shown as the following figure.

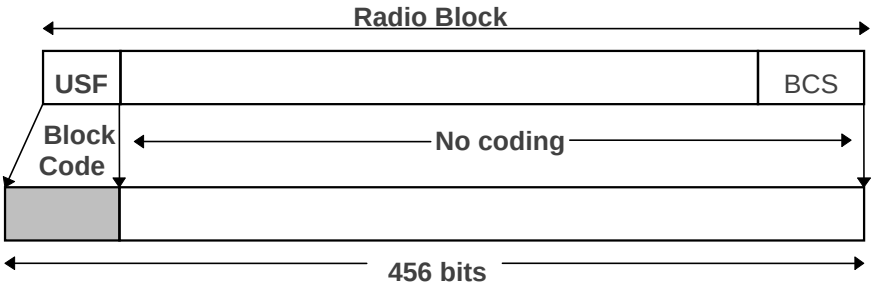

Figure 50: Radio Block Structure of CS-4

10 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications. The description of different multi-slot classes is shown in the following table.

Table 44: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5